

Bolt Schematic

Whiskey Lake

2018/12/12

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed
TypeC: CCG4
TypeC_5V_OUT: provide external device power 5V
TypeC_PWR_IN: Provide system power via typeC connector.
8111H:Reltek LAN RTL811H
81106E:Reltek LAN RTL8106E

<Core Design>



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Title

Cover Page

Size
A3

Document Number

BOLT WHL

Rev

1

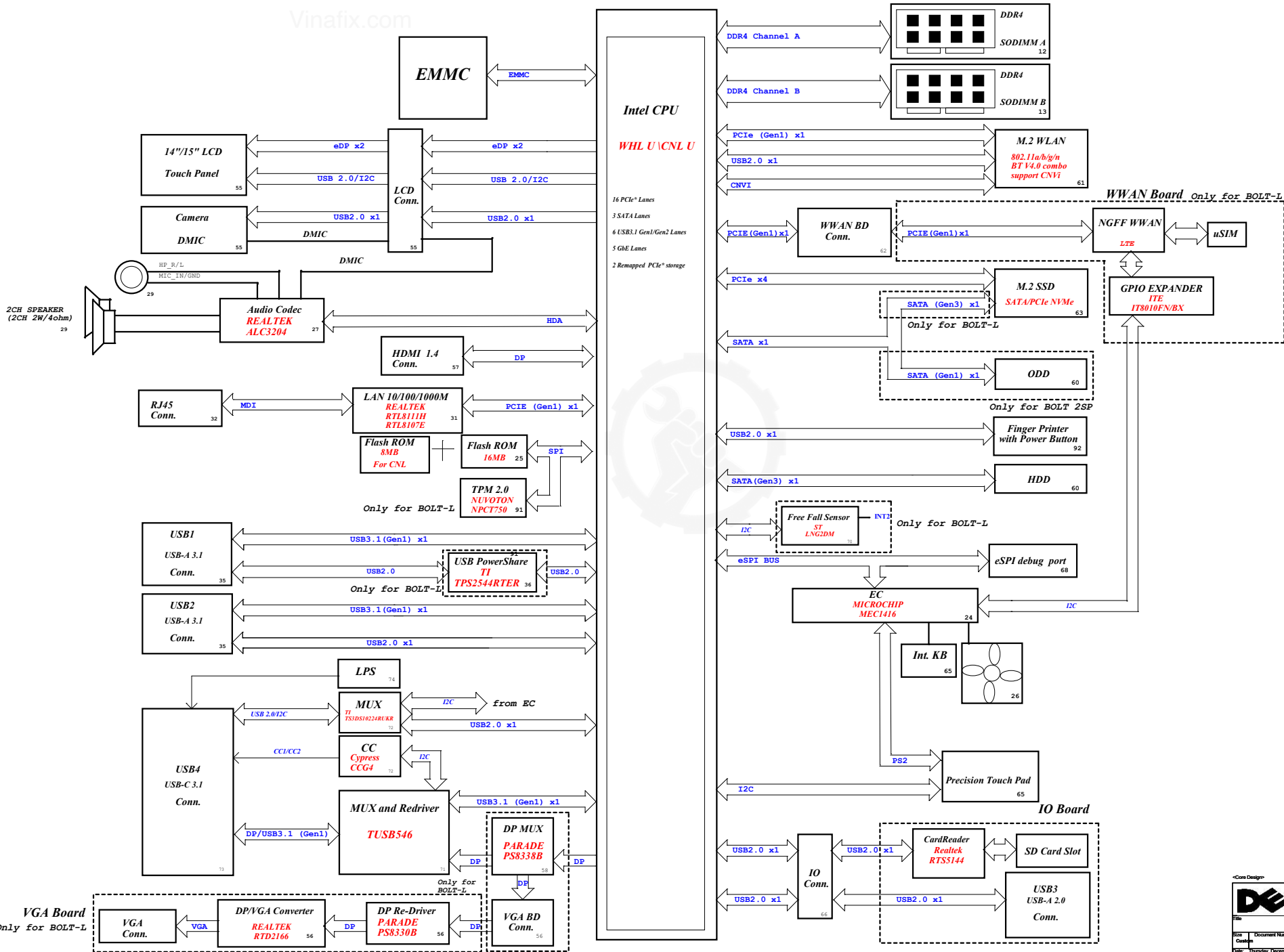
Date: Thursday, December 27, 2018

Sheet 1 of 105

Project Code : QRQY00000009
PCB P/N : 17938
Revision : 1

Bolt WHL Block Diagram

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CHARGER	
ISL95522/ISL9538	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	303V PWR 303V S5 5V PWR 5V S5
CPU Core Power	
NCPS1208MNTXG	46-50
NCPS1382MNTXG x 2	
NCPS1382MNTXG (23e)	
NCPS1253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	VCCSA
DDR4 SUS	
RT8231AGW-GP	51
APL5930KAI-TRG	
INPUTS	OUTPUTS
DCBATOUT	102V S3 100V S0 205V S3
CPU VCCPRIM_CORE 1V	
APL5930KAI-TRG	11
INPUTS	OUTPUTS
100V S5	+VCCPRIM CORE
CPU DCDC-V1D00A	
AO22262QI-10-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	100V S5
LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	OUTPUTS
303V S5	108V S5
5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	OUTPUTS
5V S5 303V S5	5V S0 303V S0
EOP10/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	OUTPUTS
100V S5 100V S5	+V EDRAM VR +V EOP10 VR
3D3V VGA	
AO3419L	86
INPUTS	OUTPUTS
303V S0	303V VGA_S0
VGA CORE	
ISL6271HRTZ-GP-U	85
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
1D5V VGA_S0	
Y8288RAC-GP	86
INPUTS	OUTPUTS
DCBATOUT	1D5V VGA_S0

Main FUNC = CPU

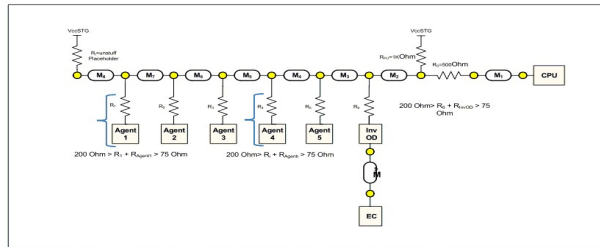
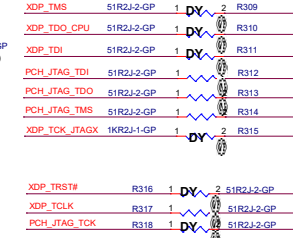


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254		254	
Topology Guidelines							
Platform resistors values		Rpu = 1KQ, Rs = 500Q, Ri + Ragent = 75-200Q, R6 + Rinvod = 75-200Q					
Platform resistors tolerances		± 5%					

Main FUNC = CPU

HDMI 1.4B

57 HDMI_DDI_TX_N0 <<<
57 HDMI_DDI_TX_P0 <<<
57 HDMI_DDI_TX_N1 <<<
57 HDMI_DDI_TX_P1 <<<
57 HDMI_DDI_TX_N2 <<<
57 HDMI_DDI_TX_P2 <<<
57 HDMI_DDI_TX_N3 <<<
57 HDMI_DDI_TX_P3 <<<
57 CPU_DP1_CTRL_CLK <<<
57 CPU_DP1_CTRL_DATA <<<
57 CPU_DP1_HPD <<<

TO DP MUX

58 DP2_DDI_TX_N0 <<<
58 DP2_DDI_TX_P0 <<<
58 DP2_DDI_TX_N1 <<<
58 DP2_DDI_TX_P1 <<<
58 DP2_DDI_TX_N2 <<<
58 DP2_DDI_TX_P2 <<<
58 DP2_DDI_TX_N3 <<<
58 DP2_DDI_TX_P3 <<<
58 DP2_AUX_CPU_P <<<
58 DP2_AUX_CPU_N <<<
58 DP2_HPD_CPU >>>

EDP

55 eDP_TX_CPU_N0 <<<
55 eDP_TX_CPU_P0 <<<
55 eDP_TX_CPU_N1 <<<
55 eDP_TX_CPU_P1 <<<
55 eDP_AUX_CPU_P <<<
55 eDP_AUX_CPU_N <<<
55 EDP_HPD >>>

24 L_BKLT_EN <<<
55 L_BKLT_CTRL <<<
55 EDP_VDD_EN <<<

61 CNVI_ENH <<<

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5.2.7 Compensation Signal Routing Guidelines

Signal	Trace Width	Termination	Resistor Value	Max Length
eDP_RCOMP	1.0mm	Series	330 Ω ±1%	500mm

5.2.8 eDP Disabling and Termination Guidelines

Signal	Trace Width	Termination	Resistor Value	Max Length
eDP_TXCPU	1.0mm	Series	330 Ω ±1%	500mm
eDP_AUXCPU	1.0mm	Series	330 Ω ±1%	500mm
eDP_HPD	1.0mm	Series	330 Ω ±1%	500mm

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Table 9-1. Pin Straps (Sheet 3 of 4)

Signal	Usage	When Sampled	Comment
SPIO_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2SD_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. Notes: 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. Notes: 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. Notes: 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RST_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVI enable. 1 = Integrated CNVI disable.

#566439

Pin Straps (Sheet 4 of 4)

Signal	Usage	When Sampled	Comment
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% Note: This strap should only be used for specific targeted 1S battery systems.
GP7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

#566439

HDMI 1.4B

TO DP MUX

HDMI_DDI_TX_N0 ALS
HDMI_DDI_TX_P0 A16
HDMI_DDI_TX_N1 A15
HDMI_DDI_TX_P1 A16
HDMI_DDI_TX_N2 AF6
HDMI_DDI_TX_P2 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6
DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE3
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2

GPU1A

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Port A

Port B

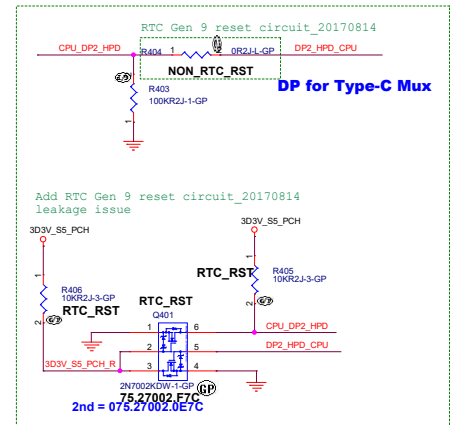
Port C

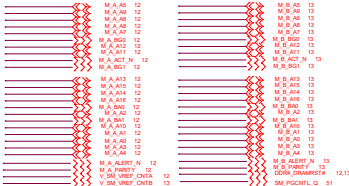
EDP_TXN0 AG4
EDP_TXN1 AG3
EDP_TXN2 AG2
EDP_TXN3 AG1
EDP_TXP0 AG4
EDP_TXP1 AG3
EDP_TXP2 AG2
EDP_TXP3 AG1
EDP_AUX_N AH4
EDP_AUX_P AH3
DISP_UTILS AM7
DDI1_AUX_N AD1
DDI1_AUX_P AD2
DDI2_AUX_N AD3
DDI2_AUX_P AD4
GPP_E13/DPB_HPD/DISP_MISC0 CM6
GPP_E14/DPB_HPD/DISP_MISC1 CM7
GPP_E15/DPB_HPD/DISP_MISC2 CM8
GPP_E16/DPB_HPD/DISP_MISC3 CM9
GPP_E17/EDP_HPD/DISP_MISC4 CM10
EDP_BKLTEN CK11
EDP_VDDEN CG11
EDP_BKLT_CTRL CH11

DP Demux

CPU_DP1_HPD CN6
CPU_DP2_HPD CN7
SIO_EXT_SMWV AG1
EDP_HPD CM10
L_BKLT_EN CK11
EDP_VDD_EN CG11
L_BKLT_CTRL CH11

add 20180512



[illegible][illegible]

Main FUNC = CPU

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15 CFG3 <<>>
15 CFG4 <<>>

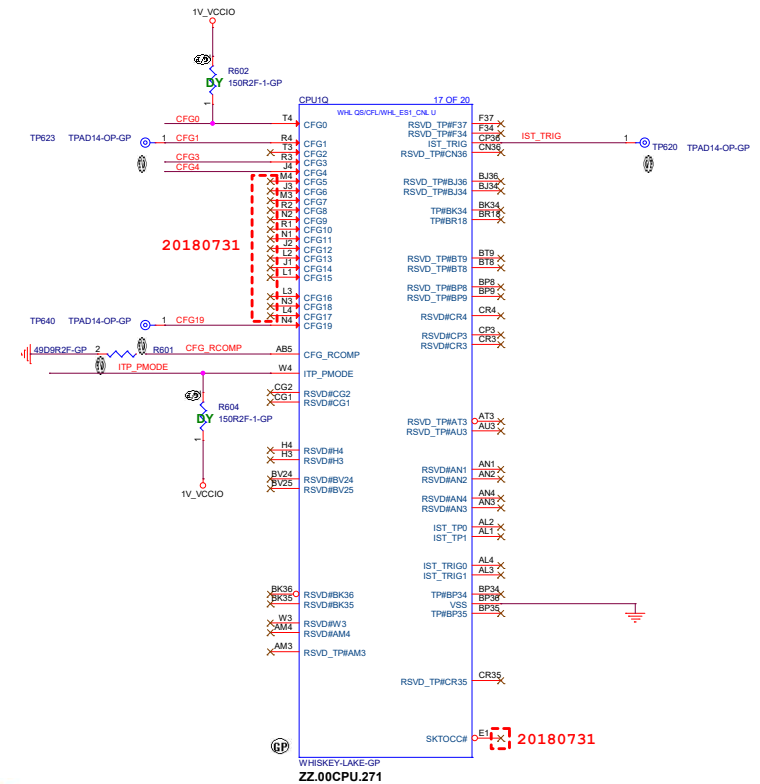


Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

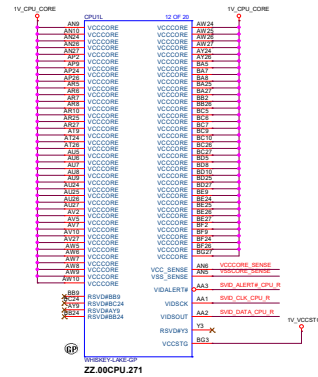
	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIe_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 162Ω ±1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

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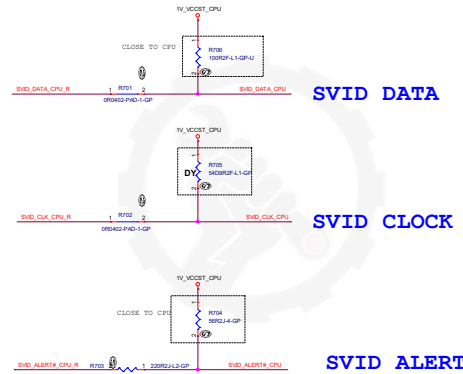
Main FUNC = CPU

46 VCCORE_SENSE
46 VCCORE_SENSE
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERTN_CPU

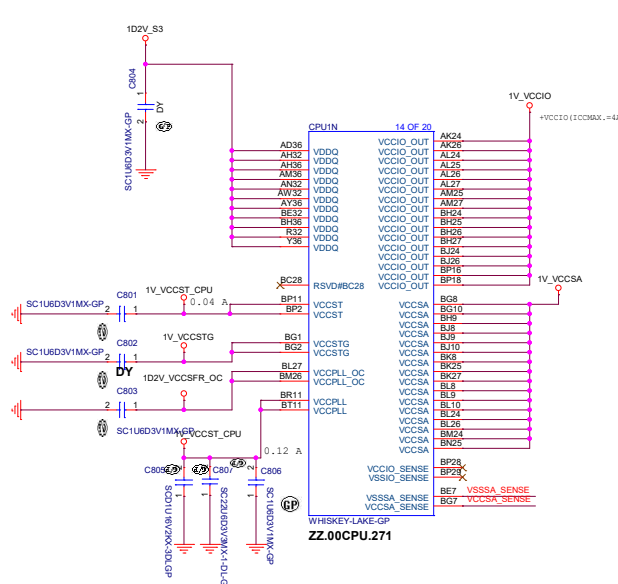
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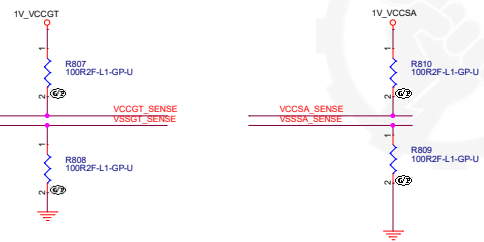
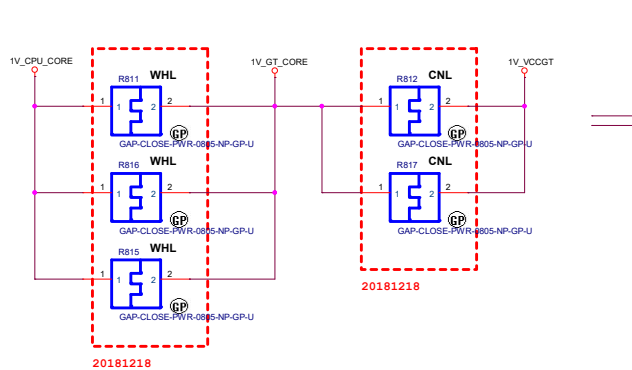
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



Main FUNC = CPU



Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



Design Target	CPU support	Stuffing options for compatibility	Incremental VR BOM vs KBL	Incremental board area vs. KBL
Cost optimized entry design (C13-SMB0-ICP)	CNL only	None	No increase expected for CNL vs. KBL U22	~0mm² vs. KBL U22
Premium design (C17-C13)	WHL only	None	Load line change anticipated to drive incremental cost vs. KBL R	TBD
Scalable mainstream design (C17-ICP)	WHL and CNL	Jumpers vary by SKU: 3 if WHL 1 if CNL	Load line change on WHL anticipated to drive incremental cost vs. KBL R No increase expected for CNL vs. KBL U22	TBD

Main Func = CPU

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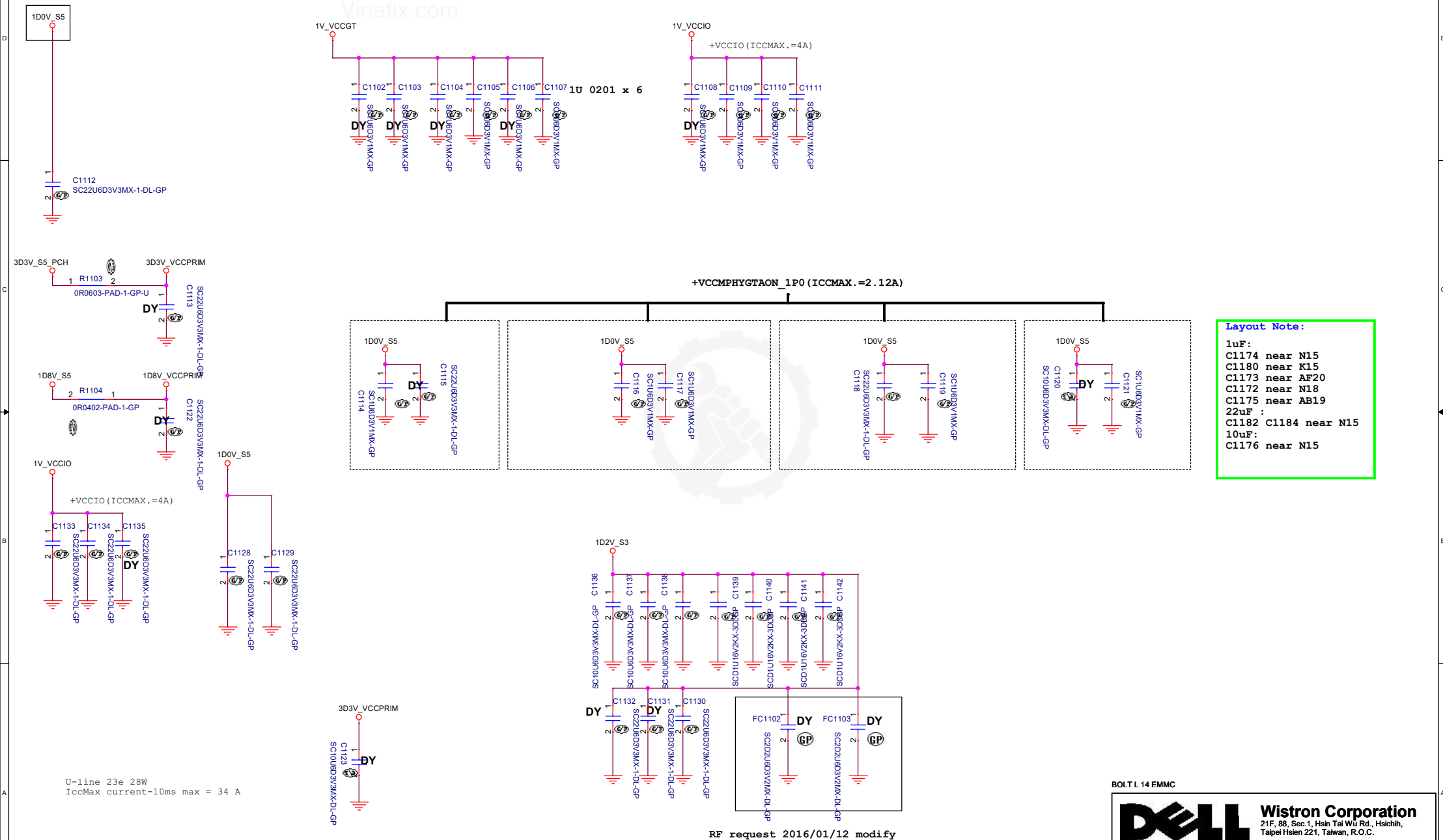


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Title (Reserved)			
Size A3	Document Number BOLT WHL		Rev 1
Date: Thursday, December 27, 2018		Sheet 9 of 105	

Main FUNC = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO

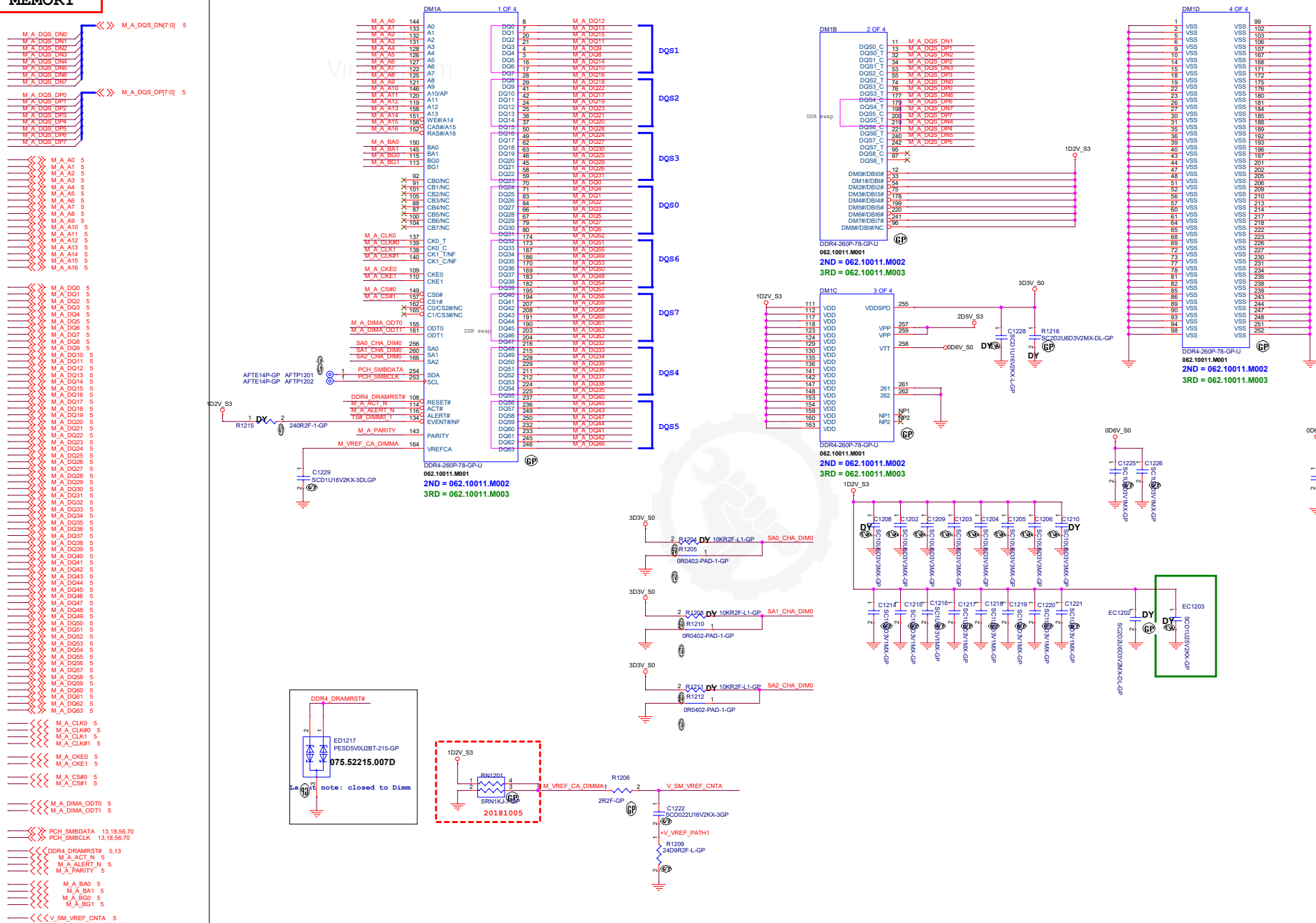


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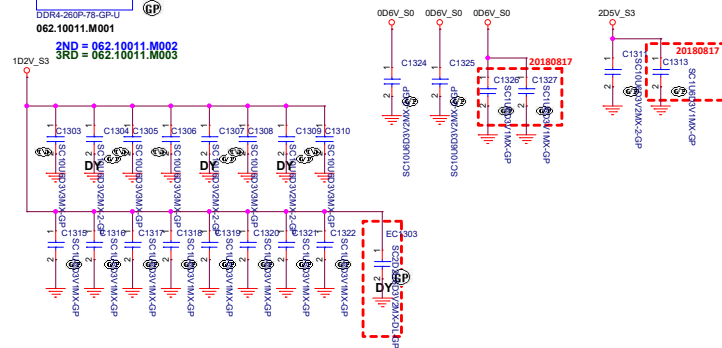
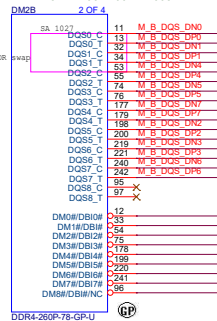
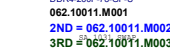
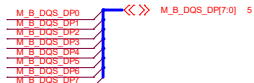
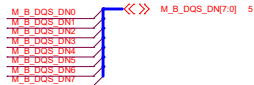


Title			
CPU_(Power CAP2)			
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Main Func
= MEMORY
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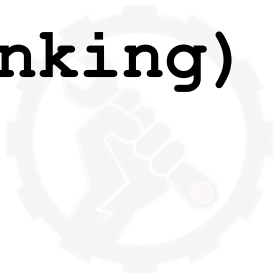
Main Func




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Title			
DDR3-SODIMM1			
Size A2	Document Number BOLT WHL	Rev 1	
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Title (Reserved)_SODIMM _SODIMM4			
Size A4	Document Number BOLT WHL		Rev 1
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GFP B18



303C88_PCH

100K2FL3-OP

301818125

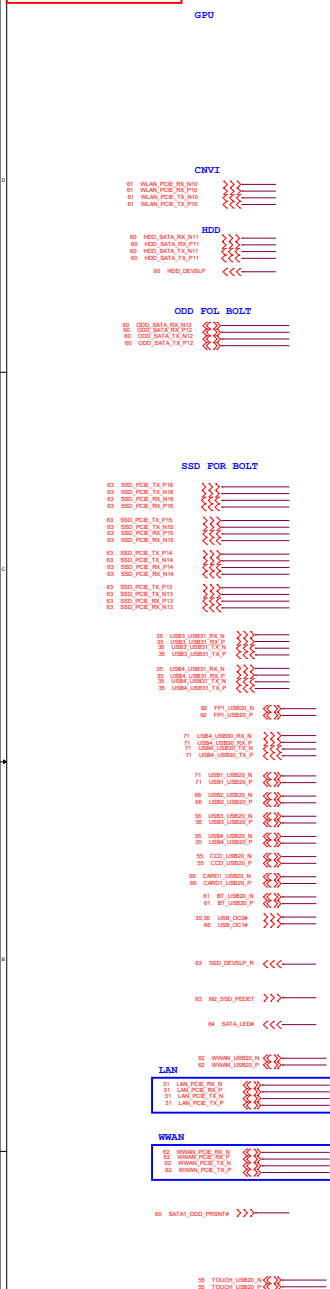
[NEW Only] PHYSICAL_SSENSE_ENABLED (EPP PRIVACY)	
CPUS[0]	0 - DISABLED SET EPP_ENABLED BIT IN SENSU INTERFACE REG 1 - ENABLED

```

(0x00000000)
DISPLAY_PORT_FREQUENCY_STOP
CPU[0]
+ 0x00000000
No external Display Port device is connected to the Extended Display Port.
+ 0x00000001 (Default)
No Physical Display Port attached to Extended DisplayPort*. So connect for disable.

```

PCH strap pin:



#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

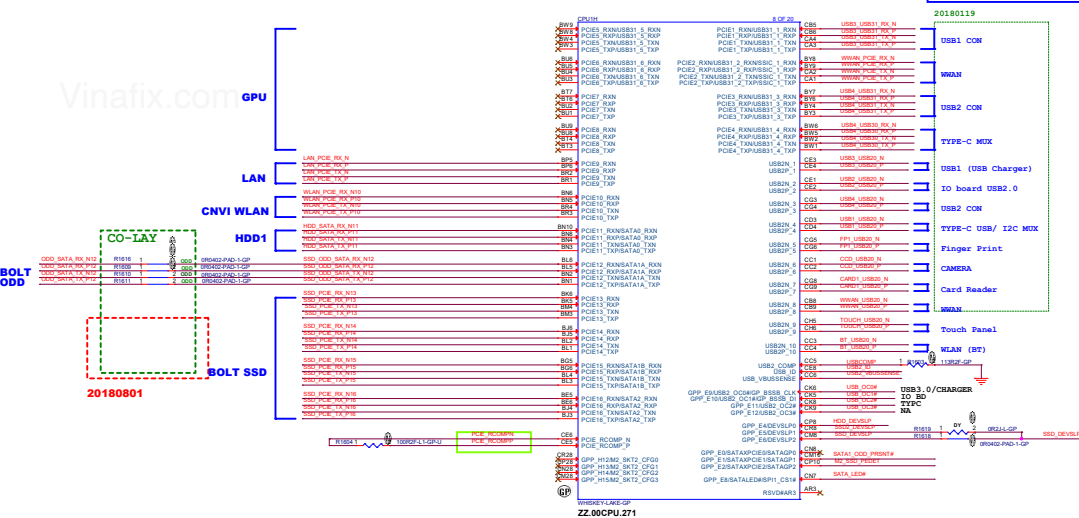


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
High Speed I/O (HSIO) Type and Lane	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	GbE	GbE	GbE	SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2	
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4.1 PCH PCI Express® Device Down Guidelines

Figure 6-3. PCH PCI Express® Device Down at 2.5, 5, and 8 GT/s Topology

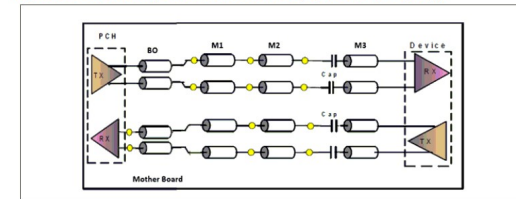
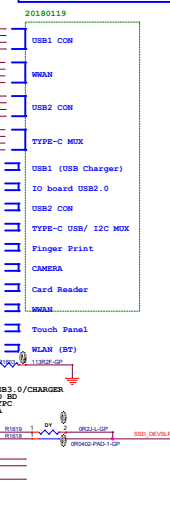


Table 6-6. PCH PCI Express® Device Down Routing Guidelines (Sheet 1 of 2)

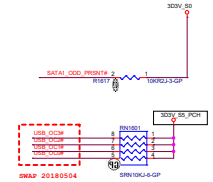
Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	BO, M1, M2, M3	MS/SL/DSL	NA	GND	GND	GND
Break-Out Max Length	BO	mm(mils)	15.2(598.42)	15.2(598.42)	15.2(598.42)	15.2(598.42)
Post-AC Capacitor Max Length	M3	mm(mils)	8(314.96)	8(314.96)	8(314.96)	8(314.96)

#543559: The xHCI controller supports USB Debug port on all USB3.0 capable ports.



USB 2.0 Table

Pair	Device
1	USB1 (USB Charger)
2	IO board USB2.0
3	USB2 CON
4	TYPE-C USB/ I2C MIX
5	Finger Print
6	CAMERA
7	Card Reader
8	WWAN
9	Touch Panel
10	LAN (BT)



Overcurrent Protection #575412

Whiskey Lake PCH has implemented programmable USB Overcurrent signals. The 4 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.1 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.

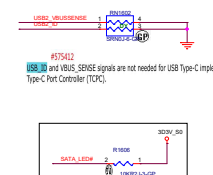
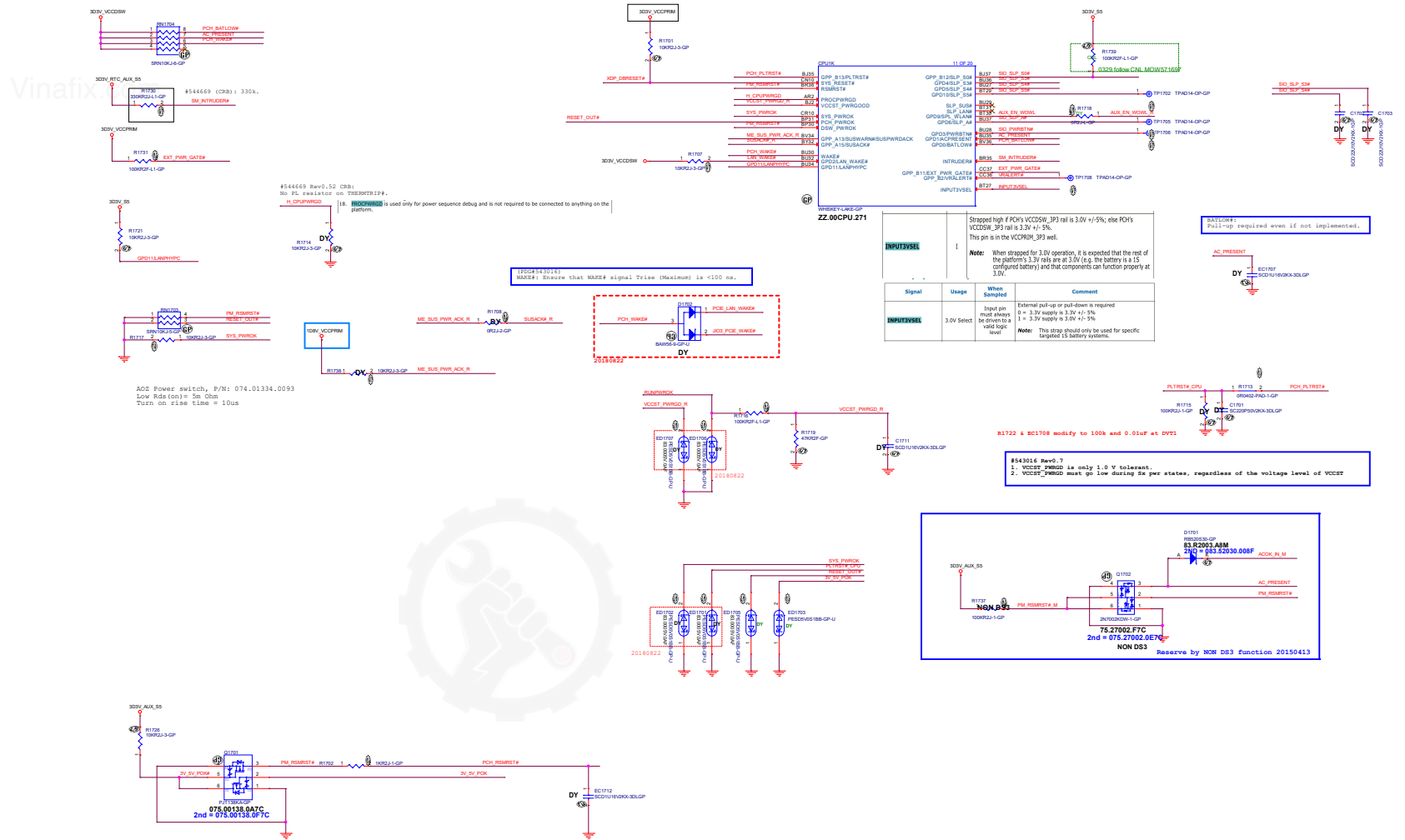


Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DORA SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIe_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 162Ω ±1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS	24.9Ω ±1% to VCCO	49.9Ω ±1% to GND	100Ω ±1% Differential	113Ω ±1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

Main Func = PC




```

25,91 SPI_0_CPU <<<
25,91 SPI_0_CPU >>>
15,25,91 SPI_0_CPU <<<
15,25 SPI_WP_CPU <<<
15,25 SPI_HOLD_CPU <<>
25 SPI_CS_CPU_N0 <<<
25 SPI_CS_CPU_N1 <<<
91 SPI_CS_CPU_N2 <<<
91 TPM_SPI_IRQ >>>

```

Diagram showing the connection of ESP1_J03 to ESP1_J00, ESP1_J01, ESP1_J02, and ESP1_J03.

PCH_SMBDATA <<>>
PCH_SMBCLK <<>>

SML1_SMBCLK <<>>
SML1_SMBDATA <<>>

```

CPU_P_4      >>>
CPU_N_4      >>>
NVME_REQ#    <<<

```

CLK_CPU_P <<< —————

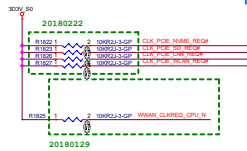
PCIE_LAN_REQ# >>> —————

CLKREQ_CPU_N <<<<
N_POE_CLK_N >>>>
N_POE_CLK_P >>>>

CPU_CLK_CPU_N <<<<
 CPU_CLK_CPU_P <<<<
 CPU_CLK_WLAN_REQ >>>>
 CPU_CLK <<<<

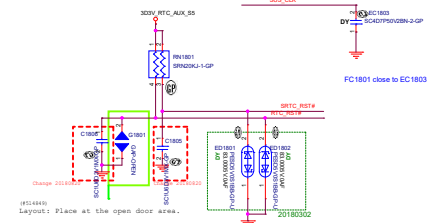
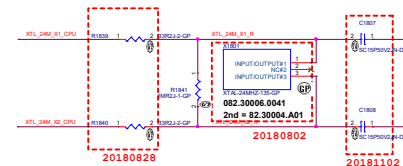
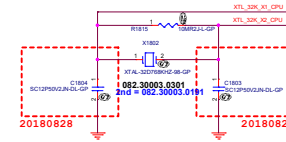
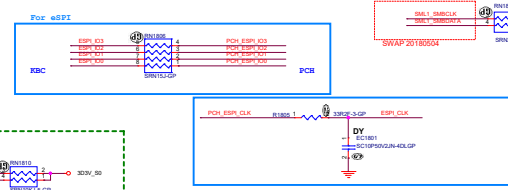
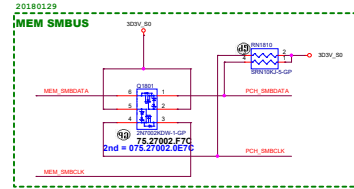
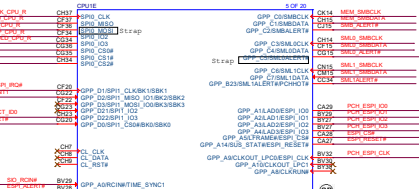
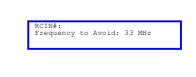
FREE FALL SENSOR

```
15 SMB_ALERT# >>>_____
15 SMD_ALERT# >>>>_____
```



Core	Component	Value
Core 1	SPT CLK CPU	10000
	SPT 3D CPU	10000
	SPT 3D GPU	10000
	SPT WP CPU	10000
	SPT HOLD CPU	10000
Core 2	SPT CLK CPU	10000
	SPT 3D CPU	10000
	SPT 3D GPU	10000
	SPT WP CPU	10000
	SPT HOLD CPU	10000
Core 3	SPT CLK CPU	10000
	SPT 3D CPU	10000
	SPT 3D GPU	10000
	SPT WP CPU	10000
	SPT HOLD CPU	10000
Core 4	SPT CLK CPU	10000
	SPT 3D CPU	10000
	SPT 3D GPU	10000
	SPT WP CPU	10000
	SPT HOLD CPU	10000

TPM
FPS
PROJE
VIDEO

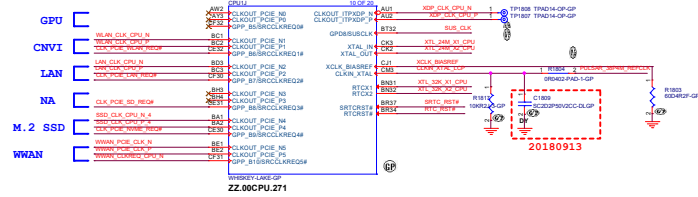


eSPI or eSPI		Table 3-1. Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash			
		eSPI Enable Strap (eSPI_EN Value (0: LPC, 1: eSPI))	Boot BIOS Strap (Boot_BIOS Value (0: SPI, 1: LPC/eSPI))	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
CPO_SMB_ALERT#_P0		0	0	LPC	SPI
		0	1	LPC	LPC
		1	0	eSPI	SPI
		1	1	eSPI	eSPI to EC over eSPI Peripheral Channel (refer to Section 3.1.4 for details)

PCH strap pin:	
eSPI or LPC	Sampled at rising edge of RSMRST#
SMB_ALERT# / GPP_CS	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.
This signal has a weak internal pull-down.	

Table 3-1. Functional Strap Definitions (Sheet 2 of 3)	
Signal	Usage
eSPI_HOSEN / GPP_B22	Boot BIOS Strap Bit Rising edge of PCH_PIOEN
SMB_ALERT# / GPP_CS	eSPI or LPC Rising edge of RSMRST#

Commit	
This signal has a weak internal Pull-down.	
This signal determines the destination of accesses to the BIOS memory. When the signal is set to 0, the Boot BIOS Destination bit (Bus, Device's, Function's, offset BCh, bit 6).	
Bit 6	Boot BIOS Destination SPI (Default)
0	1
Notes:	
1. The internal Pull-down is disabled after PLTRST# is asserted.	
2. If option 1 (SPI) is selected, BIOS may not be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot.	
3. Boot BIOS Destination value to LPC functional only when Boot BIOS Destination bit will not be integrated into PCH.	
4. The signal is in the primary view.	
This signal has a weak internal Pull-down.	
1 = LPC is selected for EC. (Default)	
1 = eSPI is selected for EC.	
Notes:	
1. The internal Pull-down is disabled after RSMRST# is asserted.	
2. The signal is in the primary view.	



CLKIN_XTAL	I		XTAL Clock Input: Single ended integrated CNV (Connectivity) XTAL clock input
------------	---	--	--

Group	Signal Name	Description
System Management	INTRUDER#	Intruder Detect: This signal can be set to disable system if box detected open.
RTC	SR1CRST#	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed.
RTC	RTC1RST#	RTC Reset: When asserted, this signal resets register bits in the RTC well.

Parameter	Segment	Stack-up	Rule
Reference Plane	M1, M2	MS/SL/DSL	Ground
Single Ended Trace Impedance	M1, M2	MS/SL/DSL	Refer Note
Max Total Length	M1+M2	MS/SL/DSL	1000mils(25.4mm)
Resistor (R1)			60 Ohm $\pm 1.0\%$
Max Transition Via Count			2

Main Func = PCH

```

>>> eDP_FHD_DET# 55
KB BL LED
65 KB_LED_BL_DET# >>>

EDP DMIC
55 DMIC_PCH_CLK >>>
55 DMIC_PCH_DATA# >>>

CNVI
61 BT_PCMOUT_CLKREQ0 <<<
61 BT_PCMFRM_RSTN <<<

CODEC
27 HDA_SYNC_CODED <<<
27 HDA_SDOUT_CODED <<<
27 HDA_BITCLK_CODED <<<
27 HDA_SDIN0_CPU >>>
27 SPKR <<<

DEBUG PORT
68 ME_FWP_R <<<

STRAP
15 HDA_SDOUT_CPU <<<

24.62 WWAN_DB_DET# >>>

LAN CABLE
31 LOM_CABLE_DETECT# >>>

66 IO_DB_DET#_GPGPS <<<

```

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	<p>0 = Port B is not detected. ★ 1 = Port B is detected.</p>
DDPC_CTRLDATA	<p>0 = Port C is not detected. ★ 1 = Port C is detected.</p>

These two signals have weak internal pull-down.

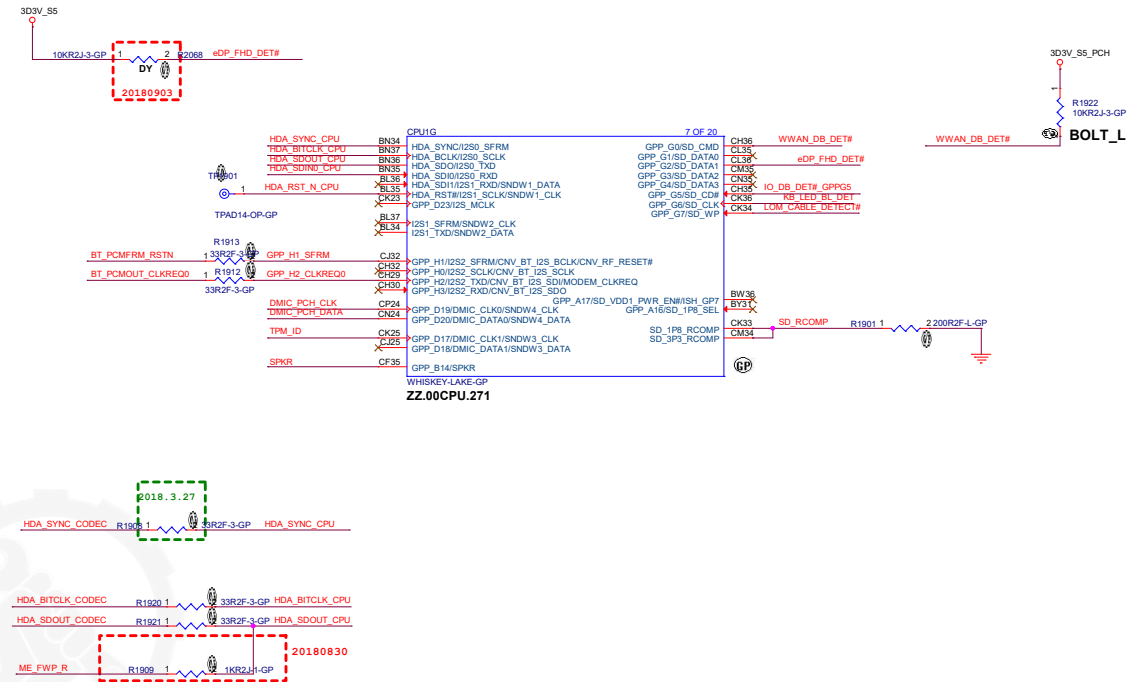
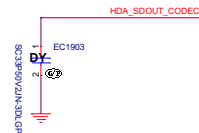
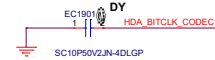
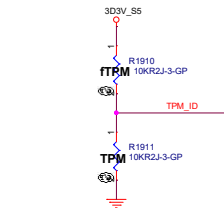
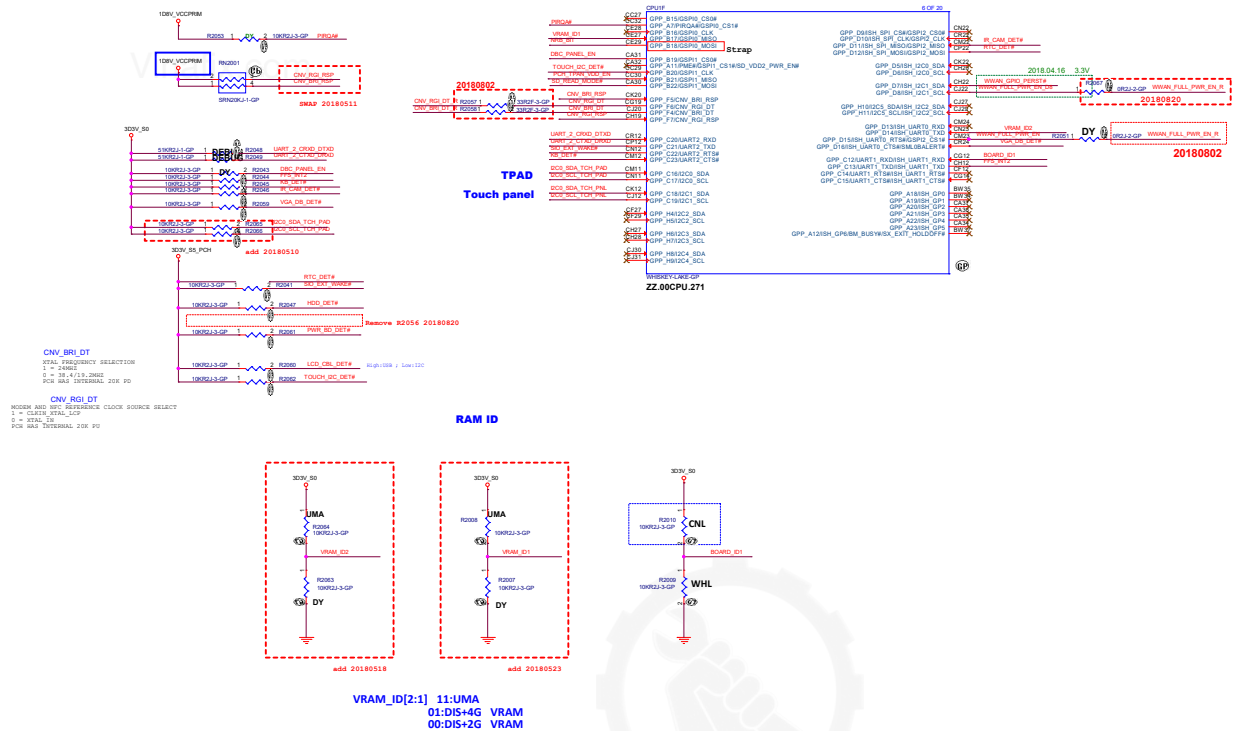


Figure 3-2. RCOMP Recommendation for WHL U42 and CFL U43e - Part 2

	SD_RCOMP_1P8	SD_RCOMP_3P3	EMMC_RCOMP	XCLK_BIASREF	CNV_WT_RCOMP	PCH_OPIRCOMP	PROC_POPIRCOMP
Board Rterm (ohm)	200Ω +/-1% to GND	200Ω +/-1% to GND	200Ω +/-1% to GND	60Ω +/-1% to GND	150Ω +/-1% to GND	49.9Ω +/-1% to GND	49.9Ω +/-1% to GND
	Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and EMMC_RCOMP can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.						
Board Rdc (ohm)	<0.1	<0.1	<0.1	<0.5	<0.5	<0.2	<0.2
SD3	X	X					
EMMC			X				
POPI						X	X
XTAL				X			
CNV1_DPHY					X		

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55	TOUCH_IC_DET#	<<<
61	CNV_BRI_RST#	<<<
15.01	CNV_RST_DET#_N	<<<
61	CNV_BRI_RST#	<<<
61	CNV_BRI_DET#_N	<<<
51	PRPWR	<<<
BOARD SETTING		
15	NRD_RST	>>>
STRAP		
SD READ CONTROL		
65	SD_READ_MODE#	<<<
DEBUG PORT		
65	UART_2_CTRD_DET#	<<<
65	UART_2_CTRD_DET#	<<<
EC		
24	SD_EXT_RESET#	>>>
KB DETECT		
65	KB_DET#	<<<
TPAD I2C IF		
65.03	SDS_SDA_TCH_FMD	<<<
65.03	SDS_SDA_TCH_FMD	<<<
PANEL		
55	SDS_SDA_TCH_FMD	<<<
55	SDS_SDA_TCH_FMD	<<<
55	SDS_SDA_TCH_FMD	<<<
55	SDS_SDA_TCH_FMD	<<<
21.05	LCD_CHL_DET#	>>>
GPU		
FREE FALL SENSOR		
70	FFS_INT2	<<<
RTC		
15.25	RTC_DET#	>>>
HDD DET		
15.00	HDD_DET#	<<<
VGA BD DET		
55	VGA_CHL_DET#	>>>
Power Button BD		
21.04	PWR_RST_DET#	>>>
55	PCH_THERM_RST_EN	<<<
62	WWAN_GPIO_RESET#	<<<
62	WWAN_FULL_PWR_EN_N	<<<



17.4.1 Configurable GPIO Voltage

Except for all pads in GPIO F group and GPD group, all other GPIO pads support per-pad configurable voltage, which allows control selection of 1.8V or 3.3V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8V level with 3.3V tolerant.
- Output: defaults to '0', except for the following GPIOs which defaults to '1' via a ~20K pull-up to 3.3V:
 - GPP_B0
 - GPP_B1
 - GPP_B11 / EXT_PWR_GATE#
 - GPP_B12 / SLP_S0#
 - GPP_H18 / CPU_C10_GATE#

A 1.8V device connected to these GPIOs must be capable of taking 20K pull-up to 3.3V.

Warning: GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

- Notes:**
 - GPIO F group supports 1.8V only.
 - GPD group supports 3.3V only.

Main Func = PCH

61 BLUETOOTH_EN <<<
61 WIFI_RF_EN <<<

20,64 PWR_BD_DET# >>>

15 GPP_H21 >>>
15 GPP_H23 >>>
15 GPD_7 >>>

40 GPPC_H18_VCCIO_LPM <<<
18 PROJECT_ID0 <<<

CNvi TX for wifi

61 CNV_WT_CLK_DP >>>
61 CNV_WT_CLK_DN >>>
61 CNV_WT_DP0 >>>
61 CNV_WT_DP1 >>>
61 CNV_WT_DN0 >>>
61 CNV_WT_DN1 >>>

CNvi RX for wifi

61 CNV_WR_CLK_DP >>>
61 CNV_WR_CLK_DN >>>
61 CNV_WR_DP0 >>>
61 CNV_WR_DP1 >>>
61 CNV_WR_DN0 >>>
61 CNV_WR_DN1 >>>

62 WWAN_BB_RST# <<<

20,55 LCD_CBL_DET# >>>

EMMC

63 EMMC_D7 <<<
63 EMMC_D6 <<<
63 EMMC_D5 <<<
63 EMMC_D4 <<<
63 EMMC_D3 <<<
63 EMMC_D2 <<<
63 EMMC_D1 <<<
63 EMMC_D0 <<<

63 EMMC_CLK >>>
63 EMMC_CMD >>>

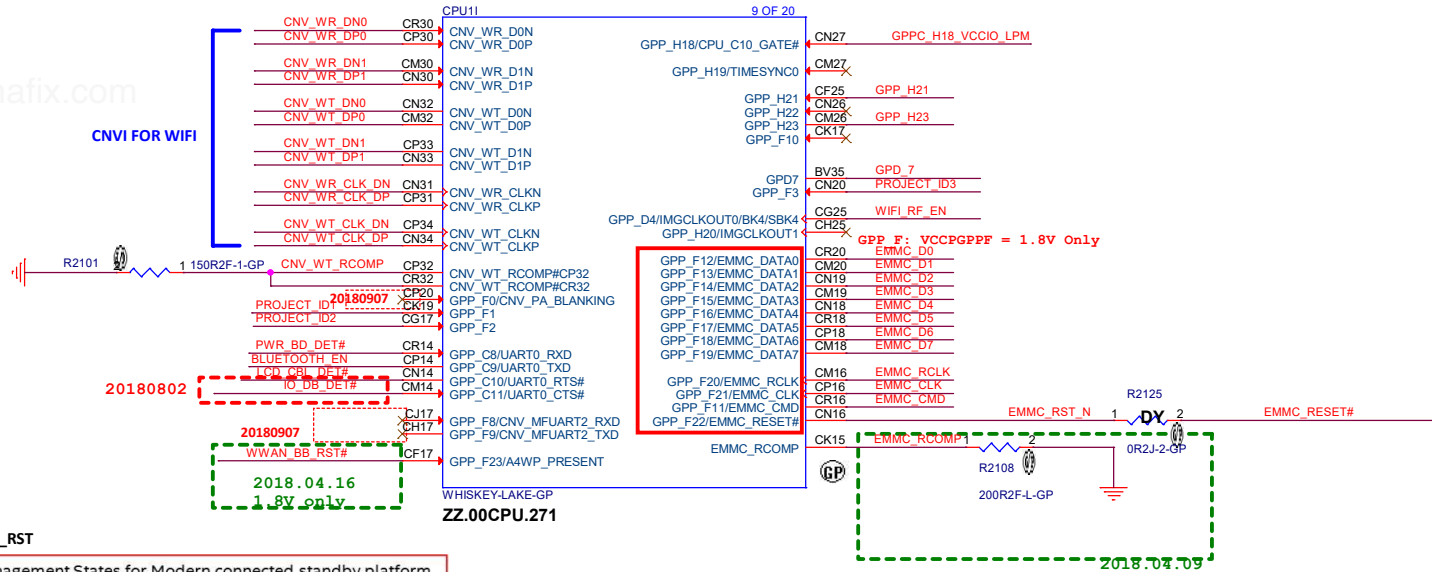
63 EMMC_RCLK <<<
63 EMMC_RESET# <<<

IO BD DET

66 IO_DB_DET# <<<

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CNVI FOR WIFI



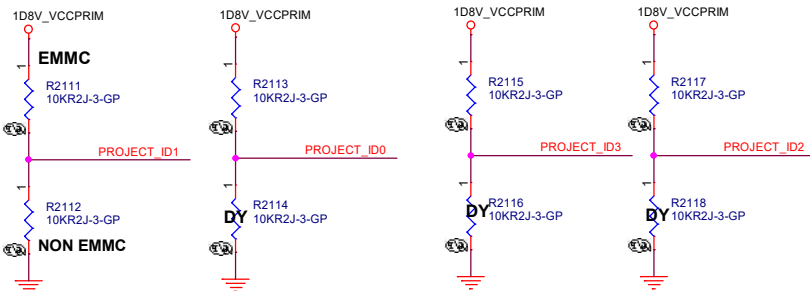
WWAN_BB_RST

Power Management States for Modern connected standby platform

System States	USB device States	PCIe device States	PCIe Link States	PERST#	PEWAKEN	CLKREQ#	BS_RESET#	Notes
S0	D0	D0	L0, L1.2	H	H	L0 : L1, L1.2 : H	H	
	D2	D3cold	L2	L	H	H	H	
S0ix	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem
S4	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	
S5	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem

PROJECT_ID[1:0] 01: 7000 Series

PROJECT_ID[3:2] 11: Inspiron

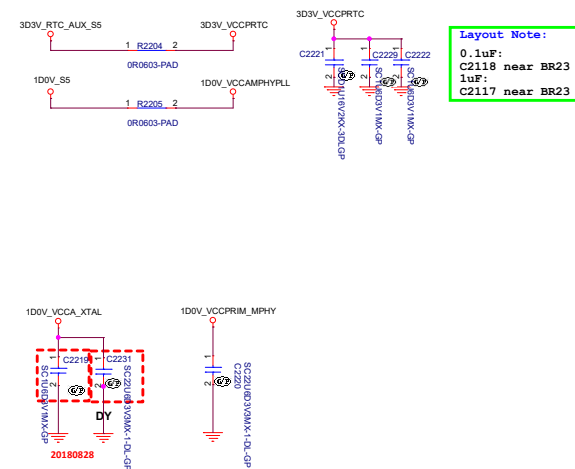
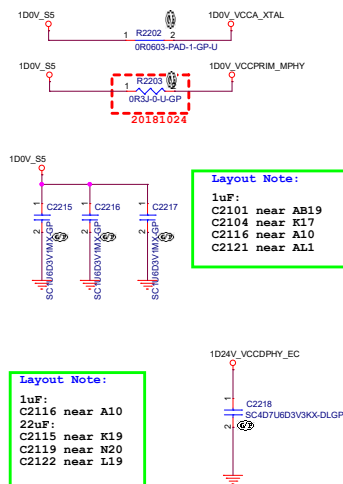
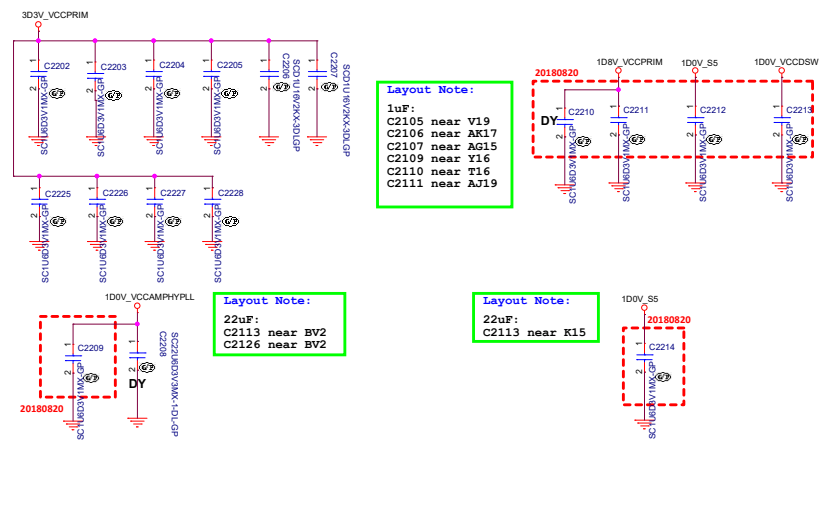
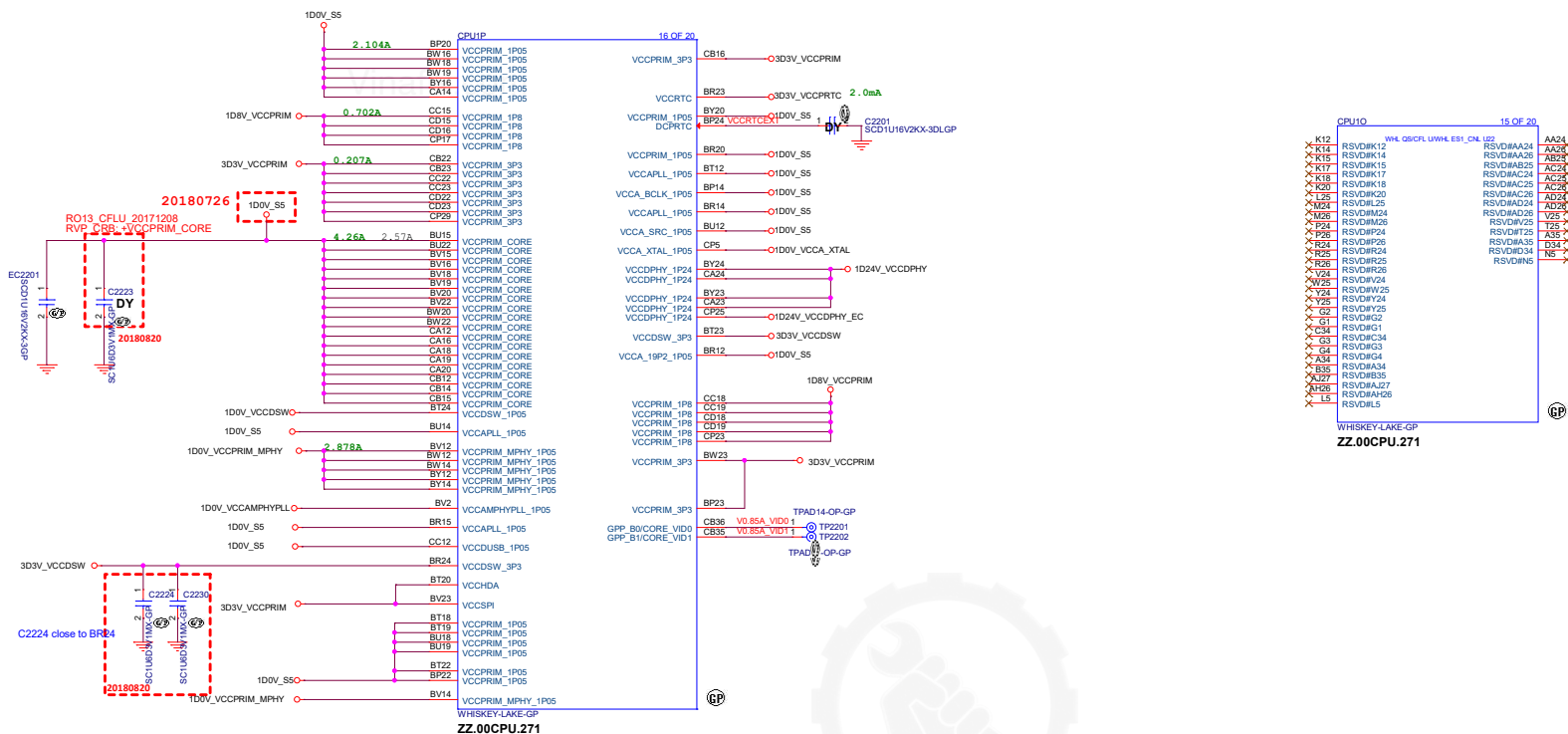


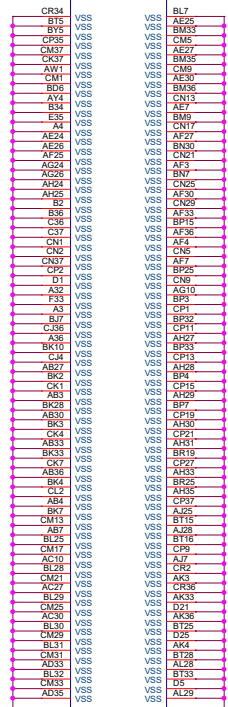
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

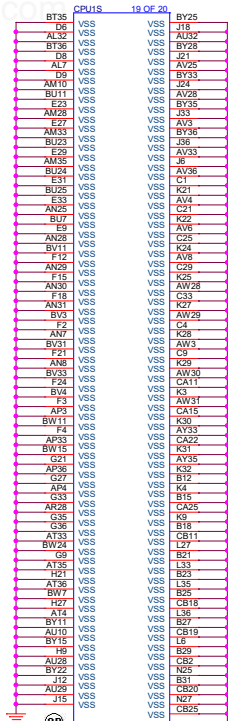
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CPU (POWER1)		
Size	Document Number	Rev
A3	BOLT WHL	1
Date:	Thursday, December 27, 2018	Sheet 21 of 105

Main Func = PCH

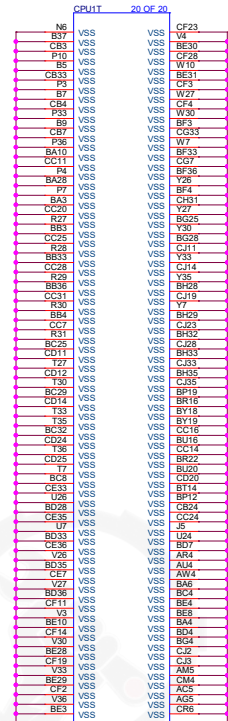




WHISKEY-LAKE-GP
ZZ.00CPU.271



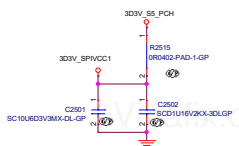
WHISKEY-LAKE-GP
ZZ.00CPU.271



WHISKEY-LAKE-GP
ZZ.00CPU.271

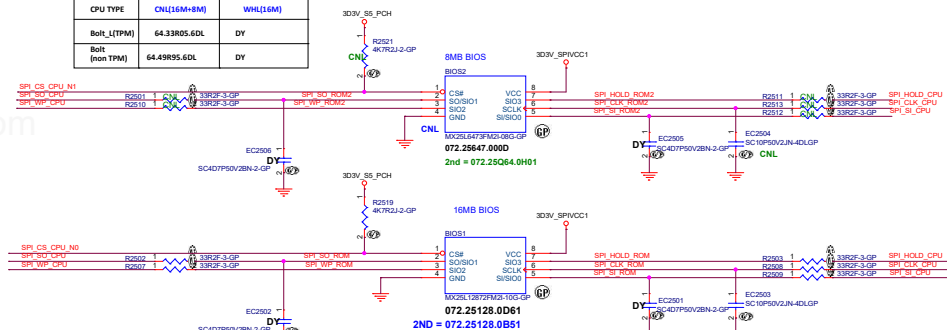
Main Func = SPI Flash

18 SPI_CS_CPU_N1 >>>
18 SPI_CS_CPU_N0 >>>
15.18 SPI_HOLD_CPU <<<
24 RTORST_ON <<<
53 3V_SV_DSW_OK <<<
18.91 SPI_WP_CPU <<<
15.18 SPI_CLK_CPU <<<
15.18.91 SPI_BI_CPU <<<
15.20 RTC_DET# <<<
24 VCCDSW_ON <<<
17.40.65 3V_SV_POK <<<



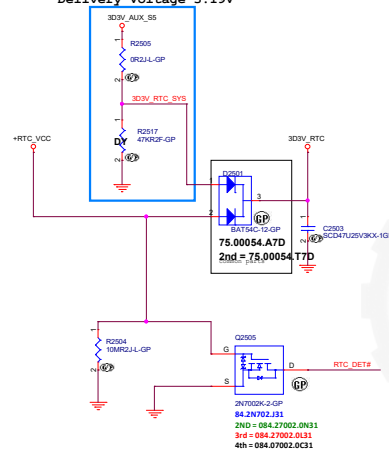
R2502/R2507/R2503/R2508/R2509			
CPU TYPE	CNL(16M+8M)	WHL(16M)	
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL	
Bolt (non TPM)	64.49R95.6DL	63.R0034.L0L	

R2501/R2510/R2511/R2513/R2512			
CPU TYPE	CNL(16M+8M)	WHL(16M)	
Bolt_L(TPM)	64.33R05.6DL	DY	
Bolt (non TPM)	64.49R95.6DL	DY	



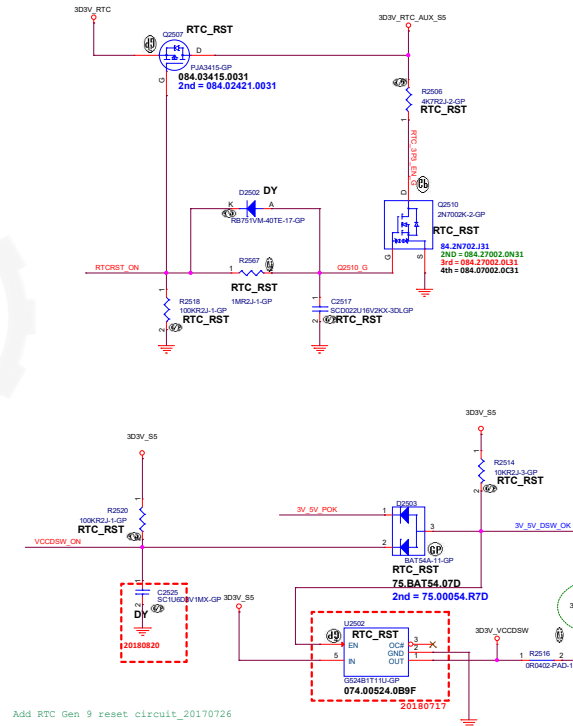
Main Func = RTC

Delivery Voltage 3.19V



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW. 3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



Add RTC Gen 9 reset circuit_20170726

BOLT L14 EMMC


```

24 FAN_TACH1 <<<<=====
24 FAN1_PWM <<<<=====

24 CMP_VOUT0 >>>>=====
24 CMP_VIND_R <<<<=====

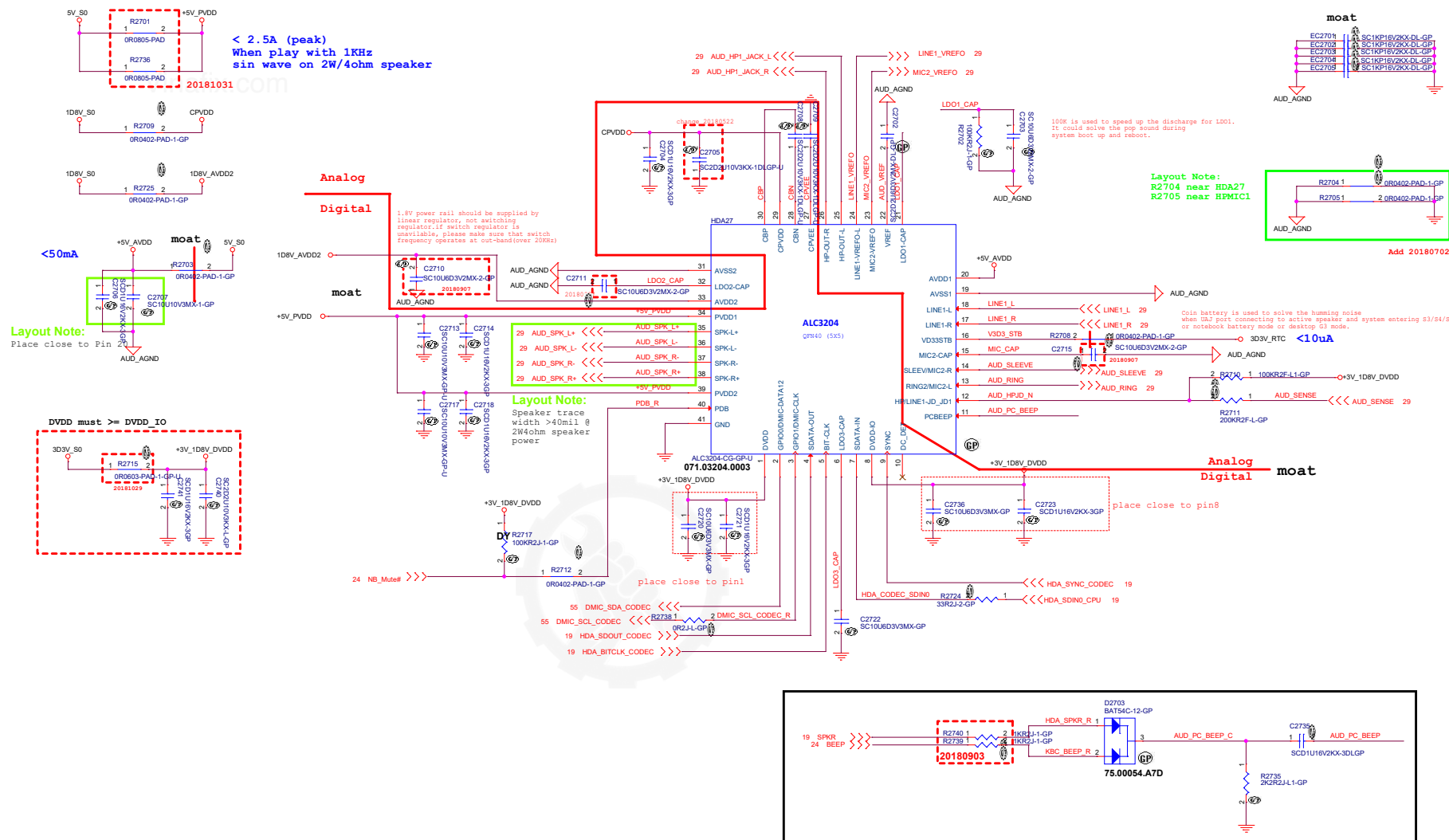
18,24 SML1_SMBDATA <<<<=====
18,24 SML1_SMBCLK <<<<=====

31,61,62,63,91 PLTRST#_CPU >>>>=====
17,24 RESET_OUT# >>>>=====
40 PURE_HW_SHUTDOWN# <<<<=====

```



Main Func = Audio



(Blanking)



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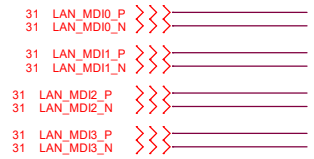
BOLT L 14 EMMC

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Title (Reserved)			
Size A4	Document Number BOLT WHL		Rev 1
Date: Thursday, December 27, 2018		Sheet 30 of	105

Main Func = LAN

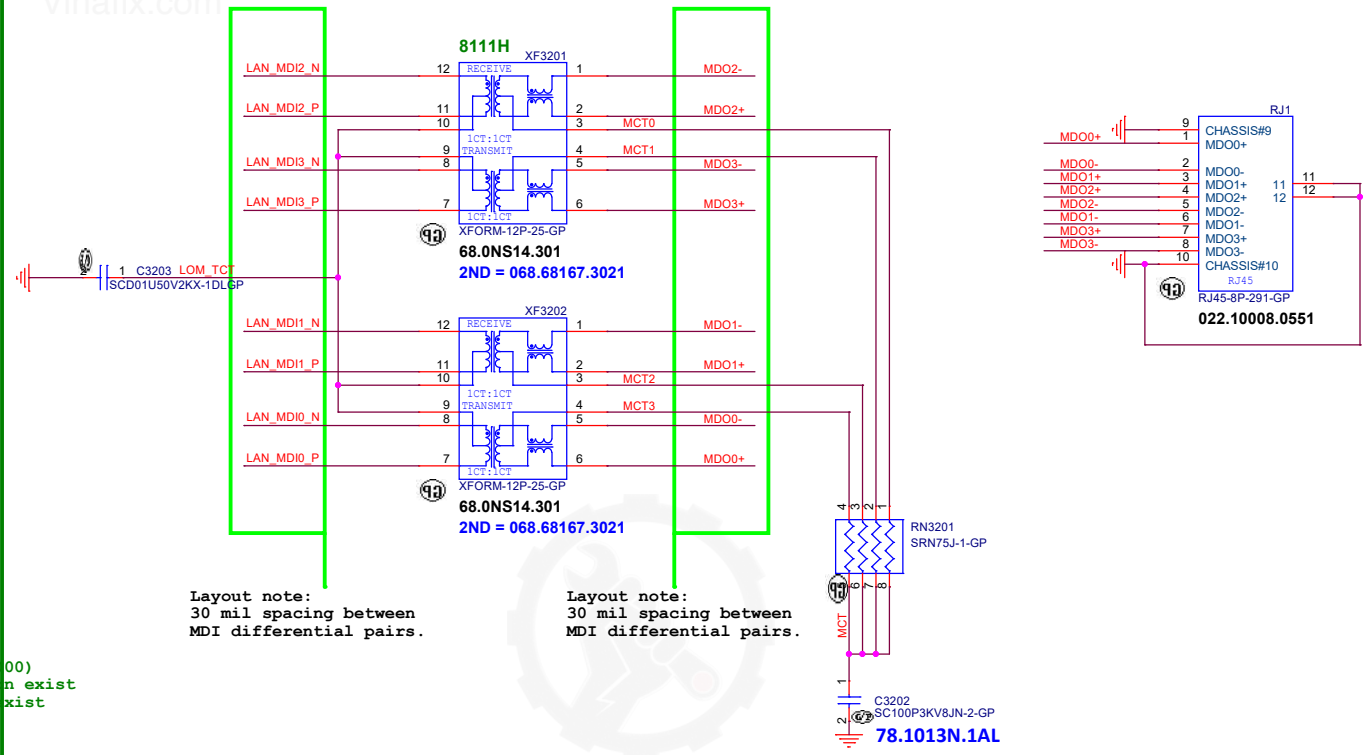
LAN TransFormer (10/100/1000M & 10/100M co-lay)

MDI

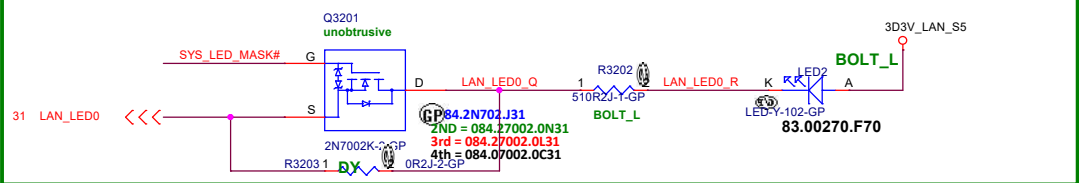


24.64 SYS_LED_MASK# >>>

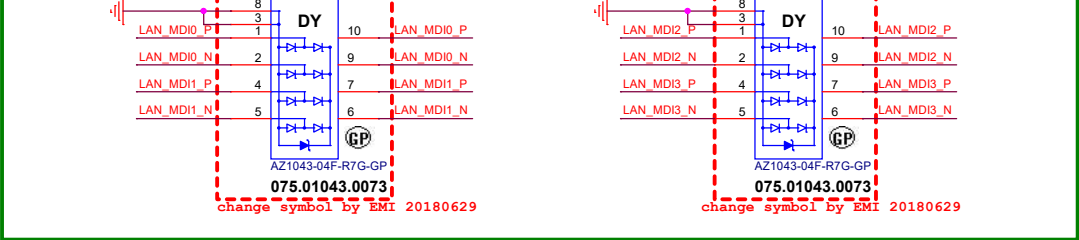
Green LED Status:
Blinking:Data transmit (10/100/1000)
Always Turn On: Network Connection exist
Turn Off: No network connection exist



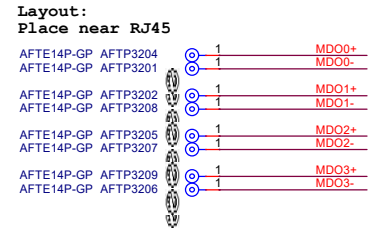
LED



LED



TEST PAD



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DELL

XFOM&RJ45

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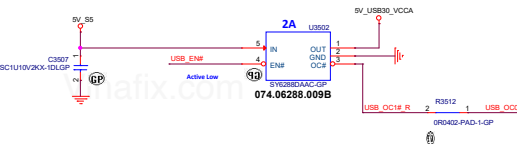
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB2.0 CONN			
Size	Document Number		Rev
	BOLT WHL		1
Date:	Thursday, December 27, 2018		Sheet 34 of 105

Main Func = USB3.0

USB Power Switch Enable



USB Power Switch



USB Power Sharing



3.1 性能範圍: 10 & 20														
型號	機殼尺寸	最大電流 (A)	最大電壓 (V)	T.C. 溫度係數 (ppm/°C)	阻值範圍					JUMPER (Ω)		JUMPER (Ω)		
					0100 Ω E4 - E6	0100 Ω E4 - E6	0100 Ω E4 - E6	0100 Ω E4 - E6	0100 Ω E4 - E6	J (Ω)	F (Ω)	J (Ω)	F (Ω)	
RT101 (R202)	1-W 20	25V	50V	<+30	—	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	0.5 A	5 Ω	20 Ω	20 Ω
RT102 (R202)	1-W 30	50V	100V	<+30	470 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	1 A	5 Ω	20 Ω	20 Ω
RT103 (R202)	1-W 40	75V	150V	<+30	—	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	1 A	2 A	20 Ω	20 Ω
RT104 (R202)	1-W 50	150V	300V	<+100	—	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	2 A	2 A	20 Ω	20 Ω
RT105 (R202)	1-W 60	150V	300V	<+100	—	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	10 Ω, 10 Ω	2 A	2 A	20 Ω	20 Ω

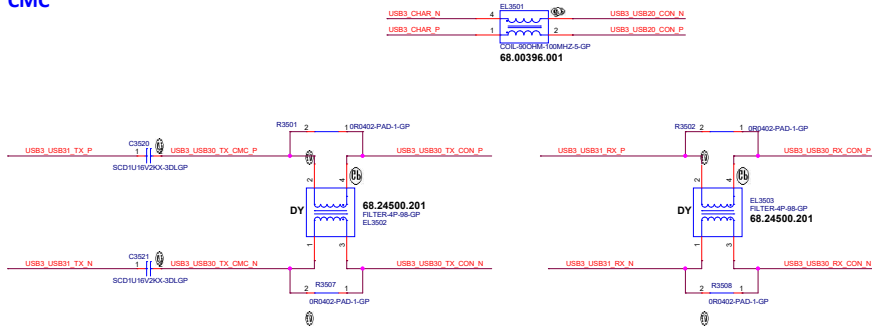
USB2.0 from USB Charger



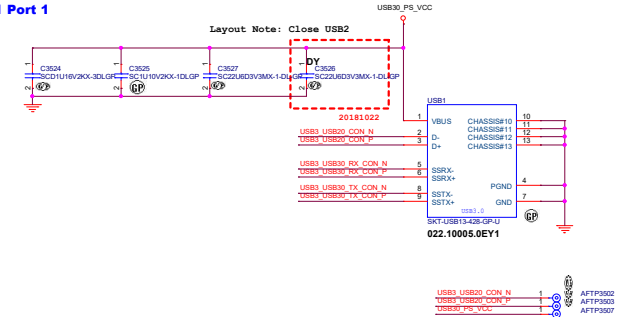
USB3.1



CMC



USB-A Connector
USB3.1 Port 1



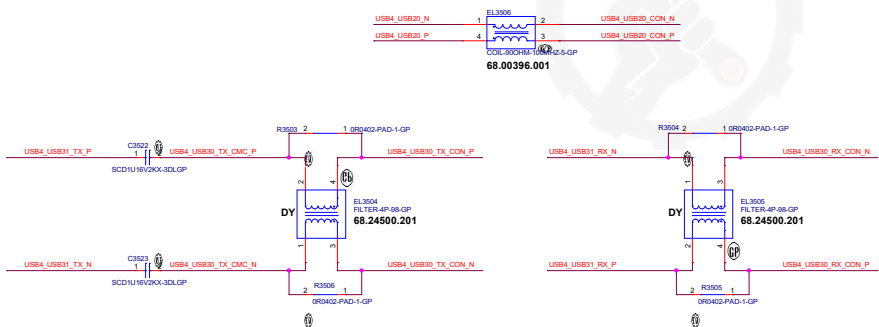
USB2.0



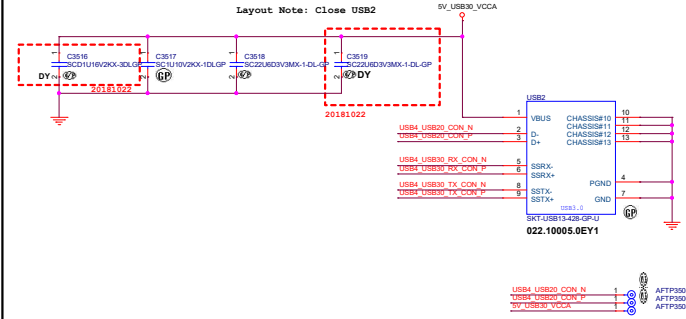
USB3.1



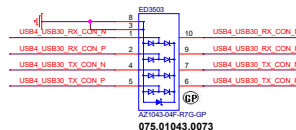
CMC



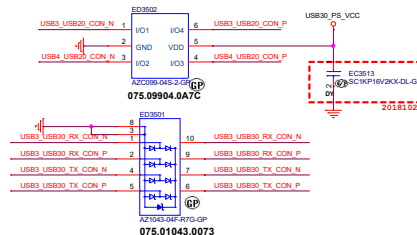
USB-A Connector
USB3.1 Port 2



ESD FOR PORT1



ESD FOR PORT2



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Title			
USB3.0 PORT			
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Title

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Size
A4

Document Number

BOLT WHL

Rev
1

Date: Thursday, December 27, 2018

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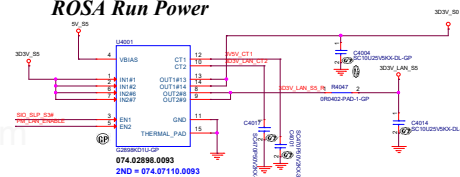


3D3V_S0/5V_S0

2018.03.28
separate 3D3V_S0/5V_S0 for layout

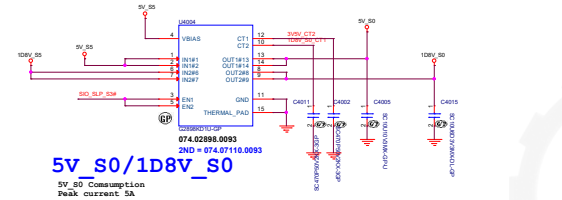
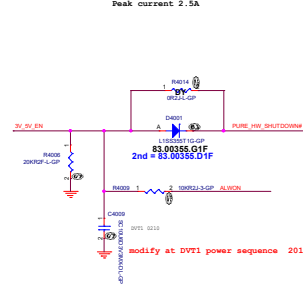
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ROSA Run Power



3D3V_S0/LAN POWER

3D3V_S0 Consumption
Peak current 2.5A



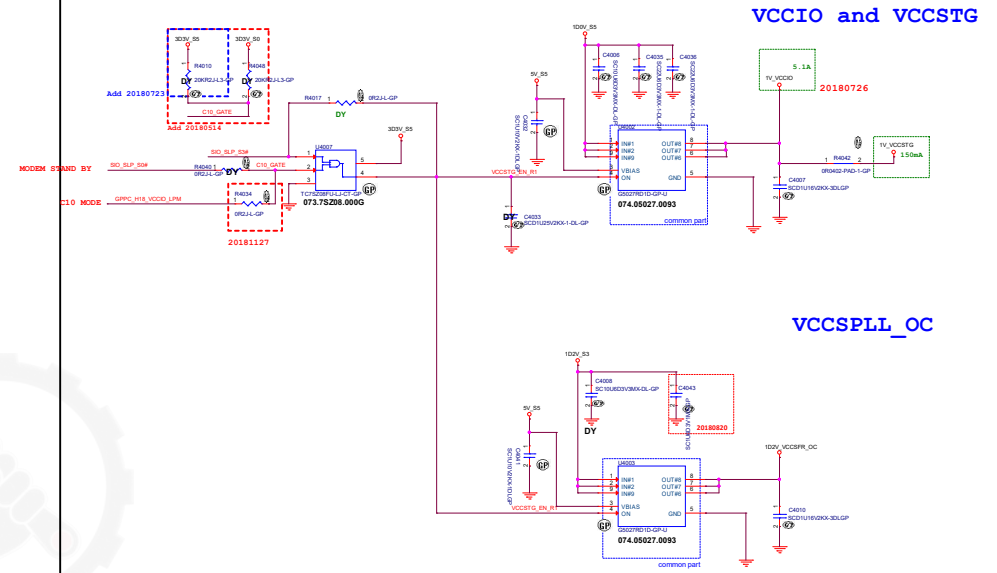
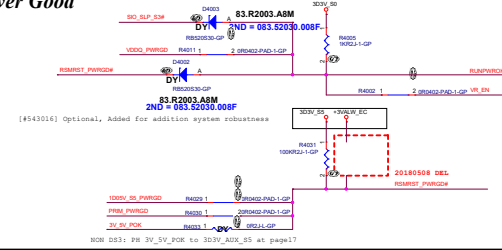
5V_S0 Consumption
Peak current 3A

Table 4. Rise Time Values

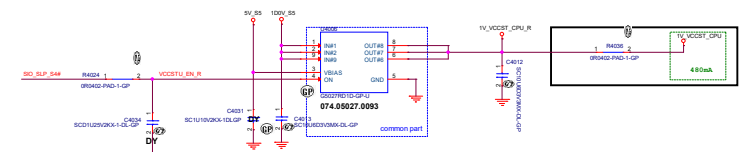
CT (pF)	RISE TIME (µs) 10% - 90%, C _L = 0.1 µF, C _{IN} = 1 µF, R _L = 10 Ω ⁽¹⁾					
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	0.6 V
0	149	112	77	70	60	56
220	548	388	236	206	173	154
470	968	673	401	342	289	256
1000	1768	1220	711	608	505	445
2200	3916	2678	1554	1332	1097	949
4700	8040	5477	3179	2691	2240	1964
10000	16520	11150	6410	5401	4430	3933

(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP

Power Good




VCCST/VCCPLL



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Title (Reserved)			
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Date: Thursday, December 27, 2018		Sheet 41 of	105

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BOLT L 14 EMMC



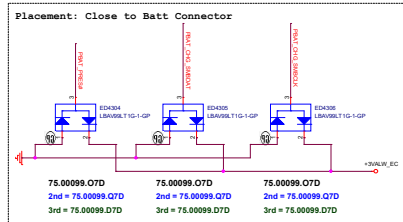
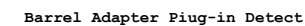
Wistron Corporation
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Title **Connected_Standby(2/2)**

Size A4	Document Number BOLT WHL	Rev 1
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Main Func = M-BAT Input



ISL9538 Buck-Boost Charger

OFF PAGE

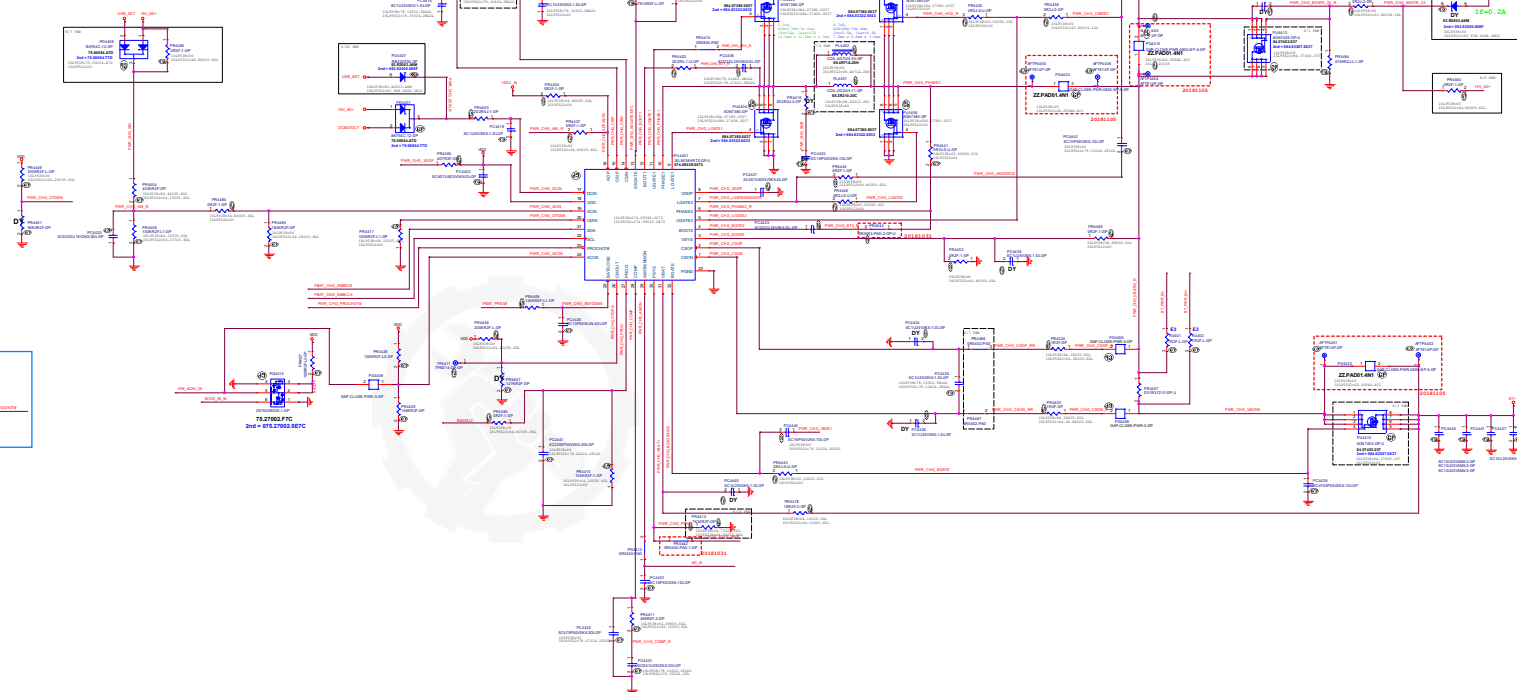
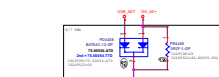
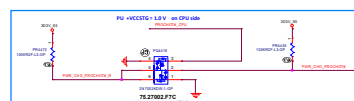
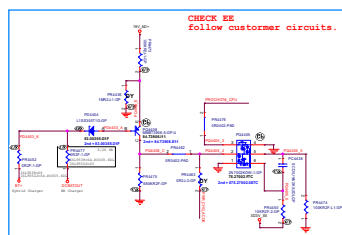
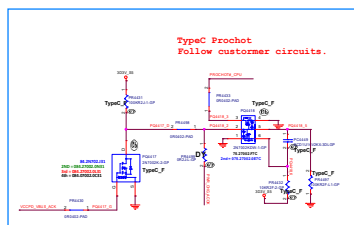
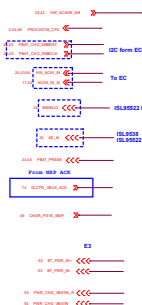
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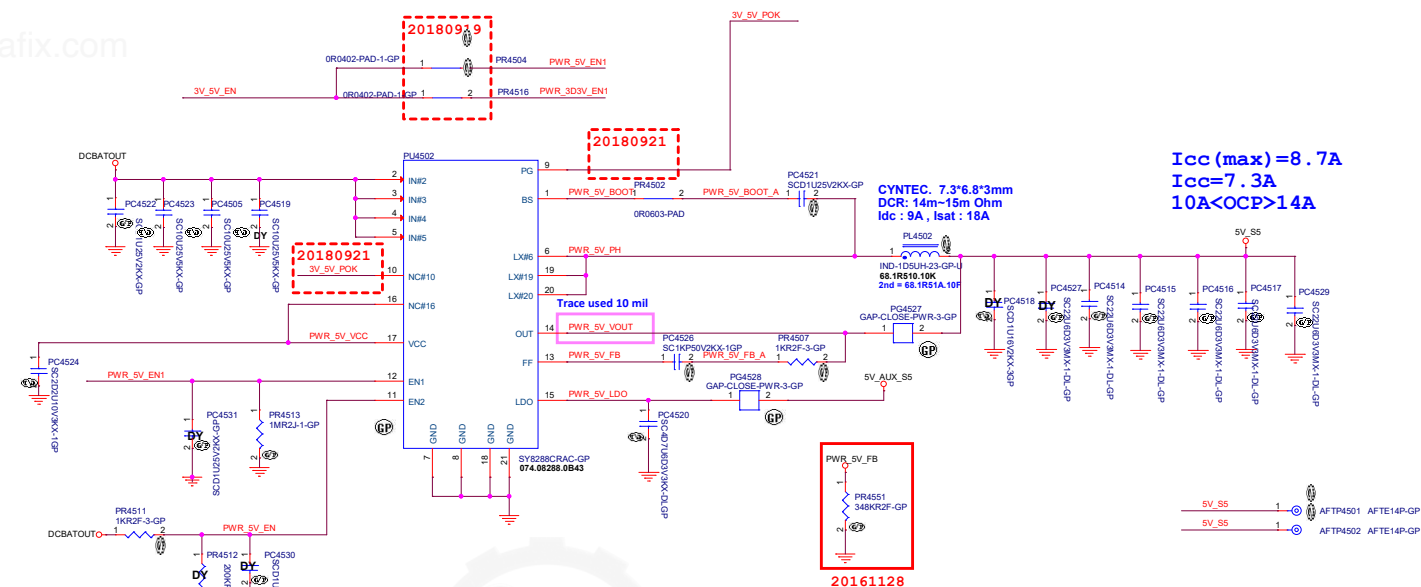
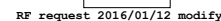
TABLE 22. PROG FIN PROGRAMMING OPTIONS

PROGRAM FREQUENCY (Hz)		TYPE	DEFAULT	DEFINITION	Autonomous	DEFAULT
MIN	MAX	CELL	7323MHz	7323MHz	Acquiring	Acquiring
8.40	8.40		7323MHz	No	1.5	1.5
14.7	14.7		7323MHz	No	1.5	1.5
25.0	25.0		7323MHz	No	1.5	1.5
26.0	26.0		7323MHz	Yes	0.476	0.476
36.7	36.7		7323MHz	Yes	1.5	1.5
43.2	43.2	2	7323MHz	Yes	1.5	1.5
62.5	62.5		7323MHz	No	0.476	0.476
69.8	69.8		7323MHz	No	0.476	0.476
71.5	71.5		7323MHz	No	1.5	1.5
82.5	82.5		7323MHz	No	1.5	1.5
83.0	83.0		7323MHz	No	0.476	0.476
105	3	7323MHz	No	1.5	1.5	1.5
118	3	7323MHz	No	0.476	0.476	0.476
133	3	7323MHz	No	1.5	1.5	1.5
142	3	7323MHz	No	0.476	0.476	0.476
156	3	7323MHz	Yes	0.476	0.476	0.476
176	3	7323MHz	Yes	1.5	1.5	1.5
215	4	7323MHz	Yes	1.5	1.5	1.5
225	4	7323MHz	Yes	0.476	0.476	0.476
231	4	7323MHz	Yes	0.476	0.476	0.476
261	4	7323MHz	No	1.5	1.5	1.5
267	4	7323MHz	No	1.5	1.5	1.5
288	4	7323MHz	No	0.476	0.476	0.476

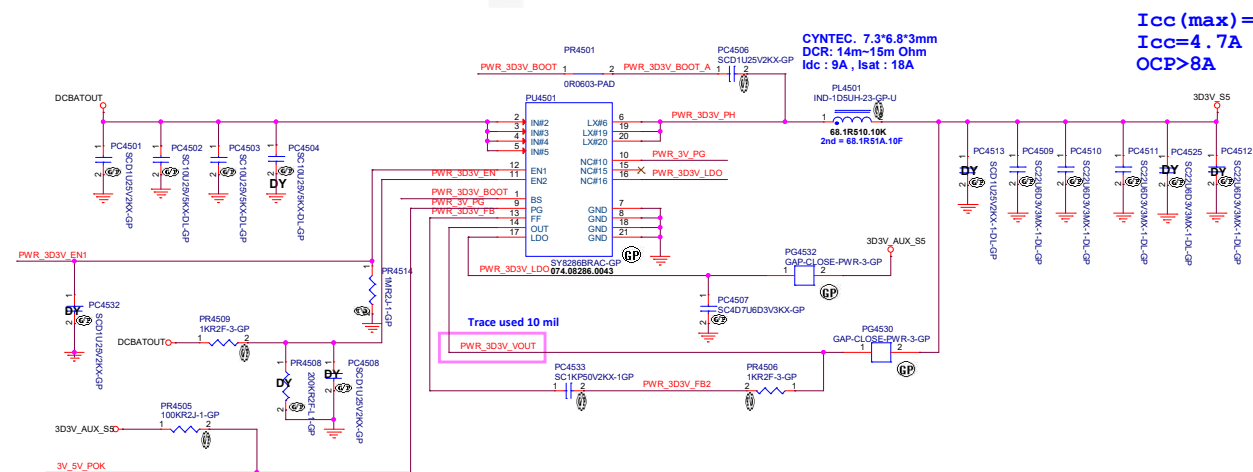
Table 17. Prog Pin Programming Options

Table 17. Ping Pin programming options			
Prog/GND Resistance (mΩ)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
Typ (1% Standard Resistor)			
22.6	0 N/DC	$R_{CS} = R_{PS} \pm 2\%$ $R_{CS} = 30m\Omega$ $R_{PS} = 30m\Omega$	3
38.3		$R_{CS} = 20m\Omega$ $R_{PS} = 10m\Omega$	2
69.8		$R_{CS} = R_{PS} \pm 1\%$ $R_{CS} = 10m\Omega$ $R_{PS} = 10m\Omega$	3
86.6		$R_{CS} = 10m\Omega$ $R_{PS} = 10m\Omega$	4
102		$R_{CS} = 10m\Omega$ $R_{PS} = 20m\Omega$	2
150		$R_{CS} = 20m\Omega$ $R_{PS} = 20m\Omega$	2
166		$R_{CS} = 20m\Omega$ $R_{PS} = 20m\Omega$	3
182		$R_{CS} = 20m\Omega$ $R_{PS} = 20m\Omega$	4
215		$R_{CS} = R_{PS} \pm 2\%$ $R_{CS} = 10m\Omega$ $R_{PS} = 30m\Omega$	4
237		$R_{CS} = 10m\Omega$ $R_{PS} = 30m\Omega$	3
255		$R_{CS} = 10m\Omega$ $R_{PS} = 70m\Omega$	2

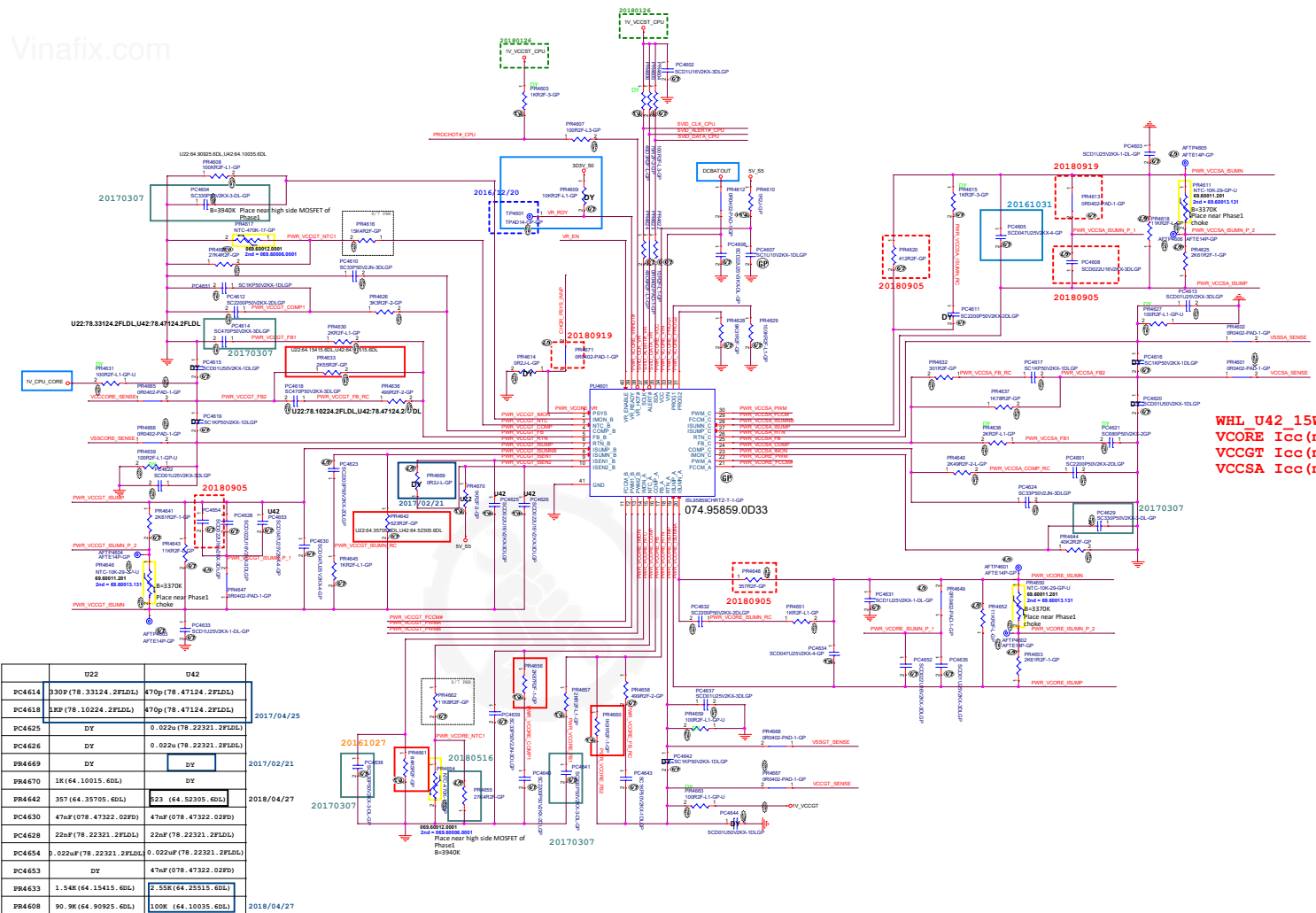

```
SSID = PWR.Plane.Regulator_3D3V
```



$I_{cc}(\max) = 8.7A$
 $I_{cc} = 7.3A$
 $10A < OCP > 14A$



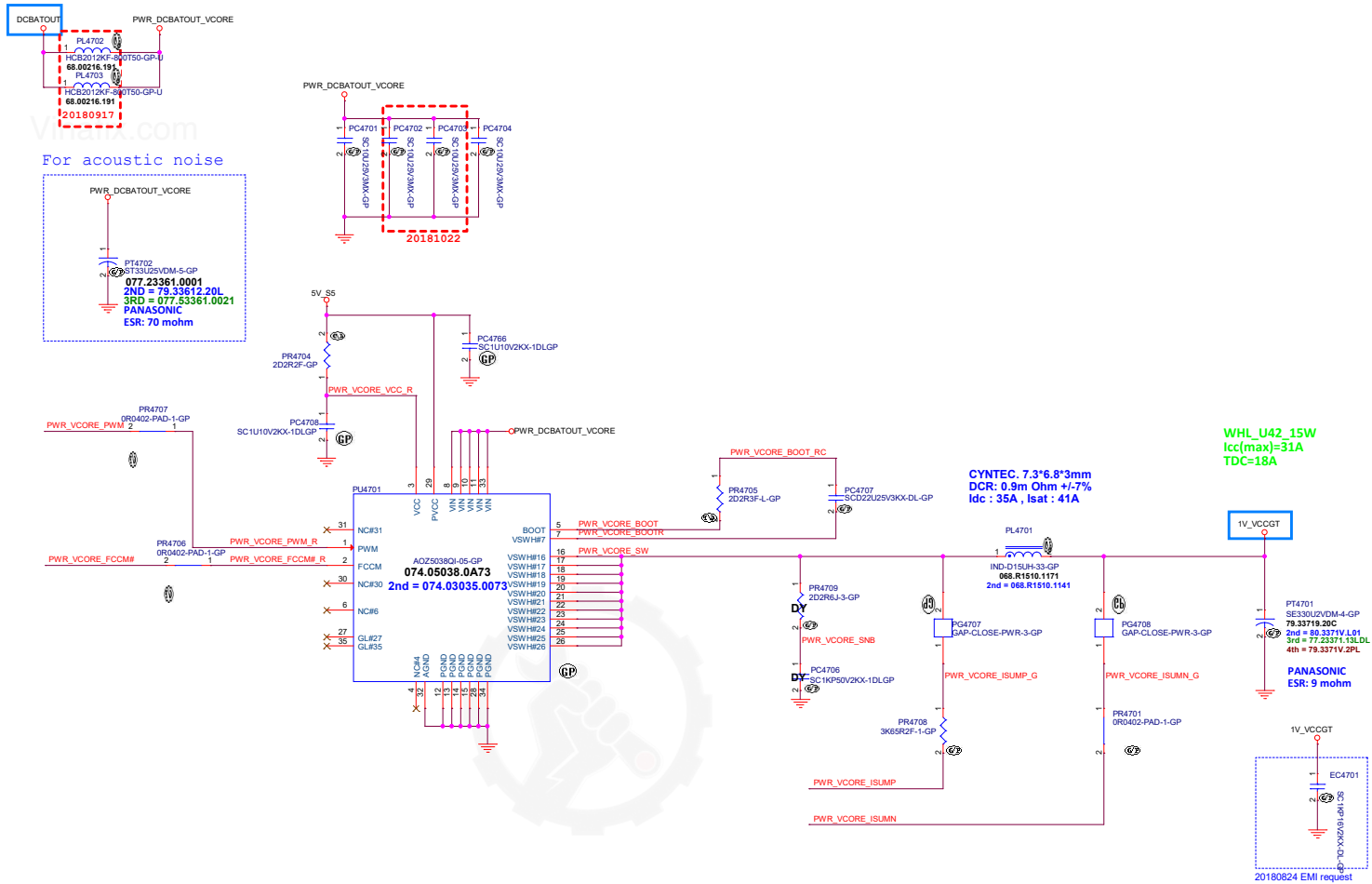
Icc (max)=7.1A
Icc=4.7A
OCP>8A



	U22	U42	
PC4614	330P (78.33124, 2FLDL)	870P (78.47124, 2FLDL)	
PC4618	8XP (78.10324, 2FLDL)	870P (78.47124, 2FLDL)	2017/04/21
PC4625	DY	0.022u (78.22321, 2FLDL)	
PC4626	DY	0.022u (78.22321, 2FLDL)	
PR4669	DY	DY	2017/02/21
PR4670	1K (64.10015, 6DL)	DY	
PR4642	35T (64.15705, 6DL)	232 (64.52305, 6DL)	2018/04/27
PC4630	47uP (078.47322, 02PDL)	47uP (078.47322, 02PDL)	
PC4628	22uP (78.22321, 2FLDL)	22uP (78.22321, 2FLDL)	
PC4654	0.022uP (78.22321, 2FLDL)	0.022uP (78.22321, 2FLDL)	
PC4653	DY	47uP (078.47322, 02PDL)	
PR4633	1.54K (64.15415, 6DL)	2.55K (64.25515, 6DL)	
PR4608	90.98 (64.90925, 6DL)	100K (64.10035, 6DL)	2018/04/27

Main Func = CPU_CORE

46 PWR_VCORE_PWM >>>
46 PWR_VCORE_FCCM# <<<
46 PWR_VCORE_ISUMP <<<
46 PWR_VCORE_ISUMN <<<



<Core Design>

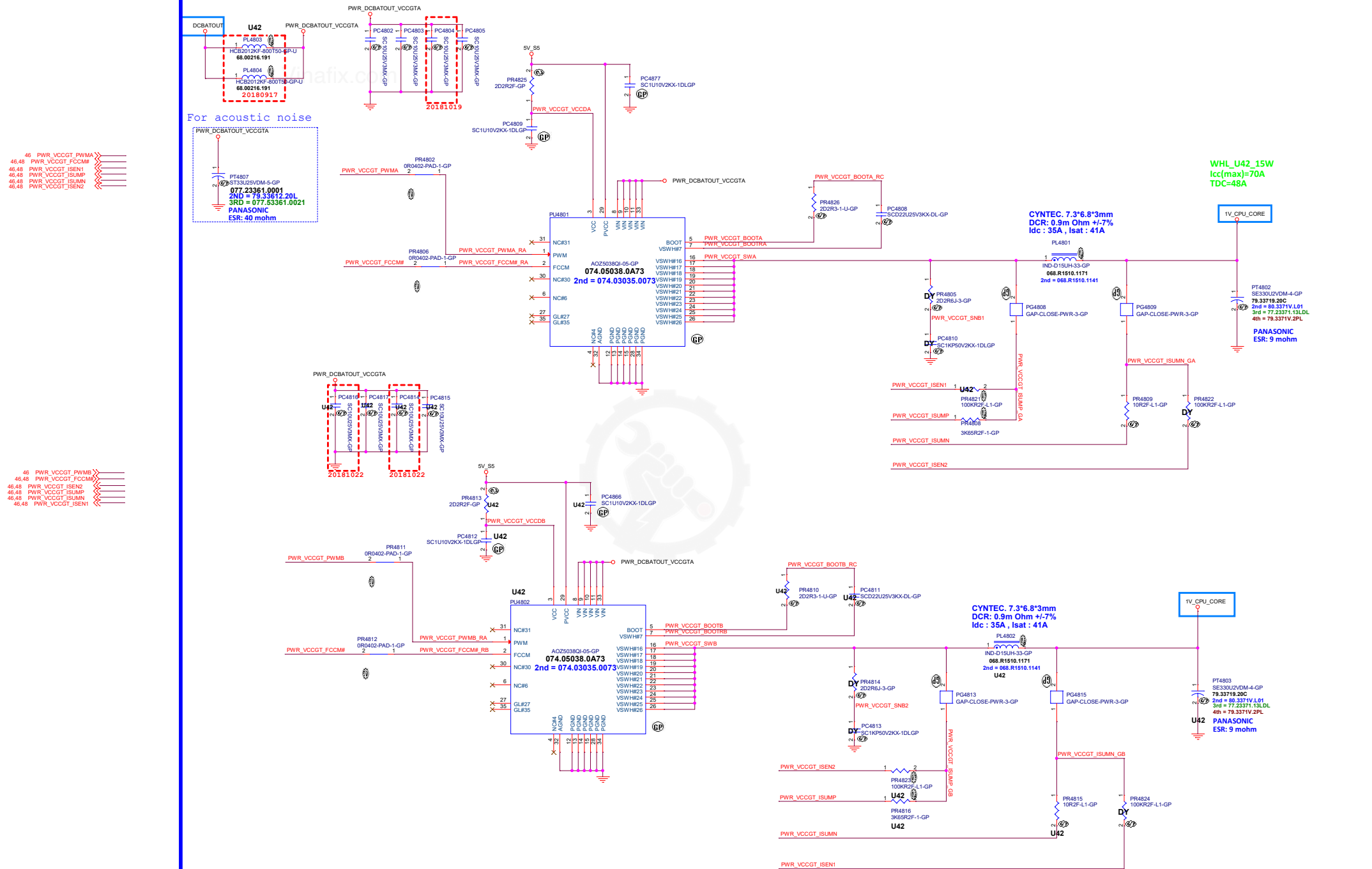
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipex Hsien 301, Taiwan, R.O.C.

Title **NCP81382MN CPU_VCORE(2/3)**

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Date: Thursday, December 27, 2018 Sheet 47 of 105

Main Func = CPU CORE



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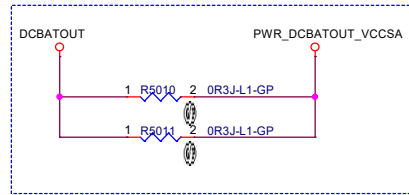
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **NCP81210MN_CPU_VCCGTUS**

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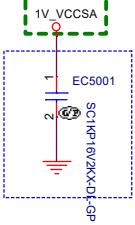
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Bolt 20180412 E3 support

PWR_DCBATOUT_VCCSA 1
AFTE14P-GP

20180126

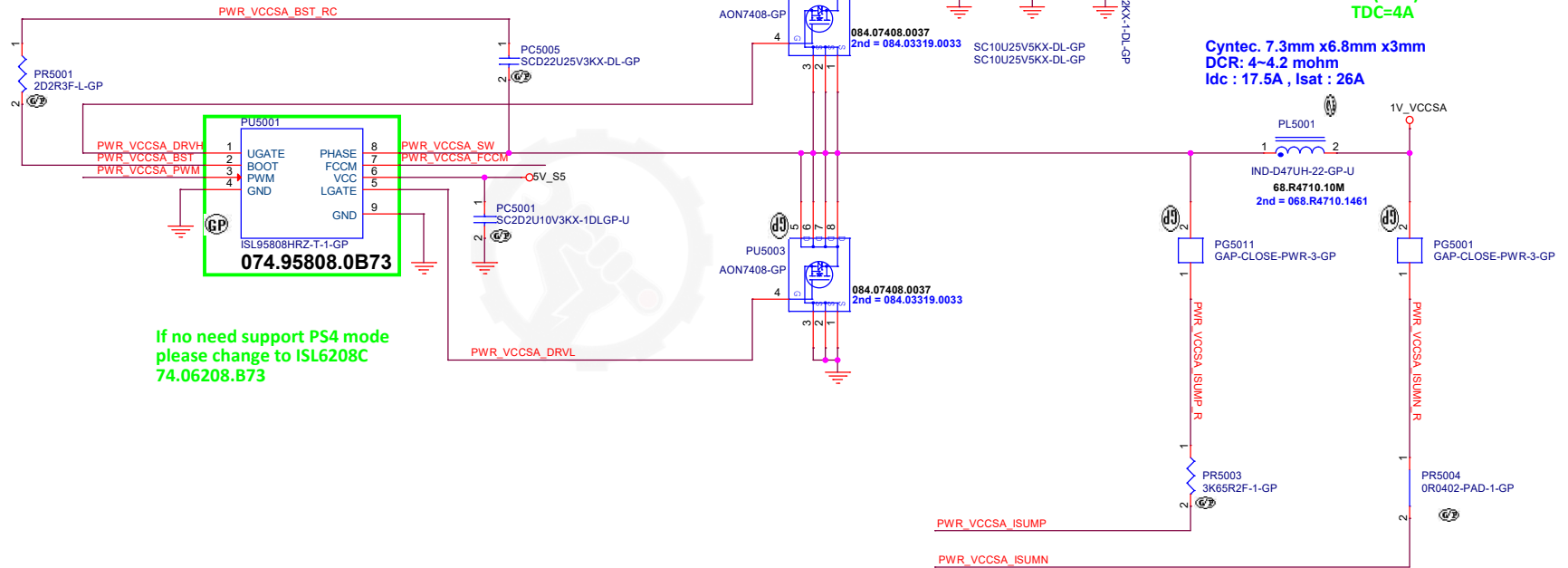


20180824 EMI request

WHL_U42_15W
Icc(max)=6A
TDC=4A

Cyntec. 7.3mm x6.8mm x3mm
DCR: 4~4.2 mohm
Idc : 17.5A , Isat : 26A

46 PWR_VCCSA_PWM
46 PWR_VCCSA_FCCM
46 PWR_VCCSA_ISUMP
46 PWR_VCCSA_ISUMN



If no need support PS4 mode
please change to ISL6208C
74.06208.B73

BOLT L 14 EMMC

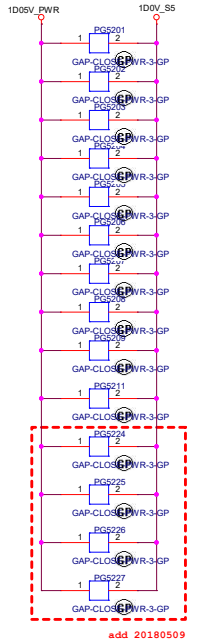
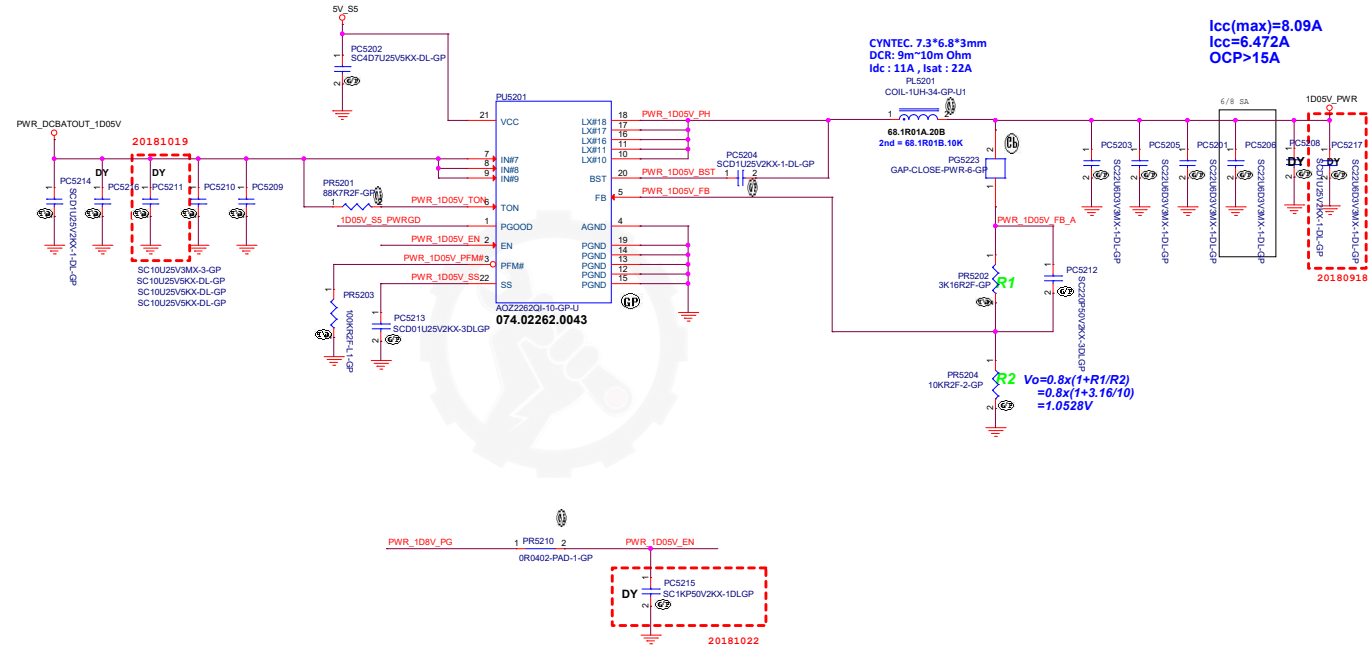
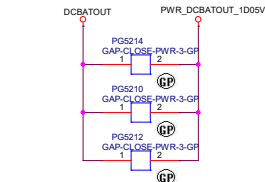


Title			
VCCSA			
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AOZ2262 for 1D05V

40 1D05V_SS_PWRGD <<<<
53 PWR_1D0V_PG >>>>



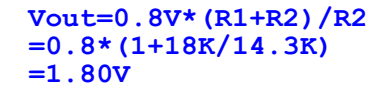
BOLT L 14 EMMC

Main Func = 1D8V

OFFPAGE GAP



$I_{CC}(\text{max}) = 1082\text{mA}$



Title				1D8V			
Size	Document Number						Rev
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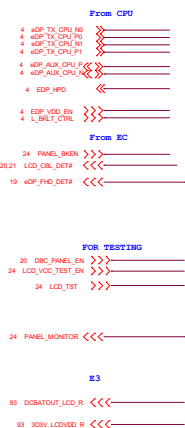
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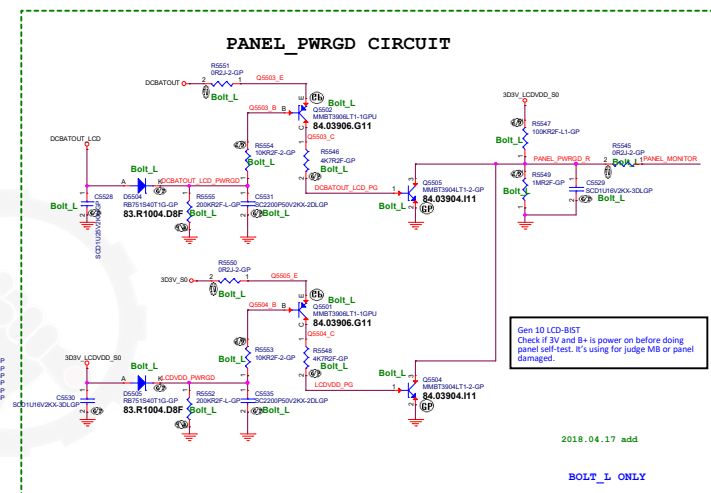
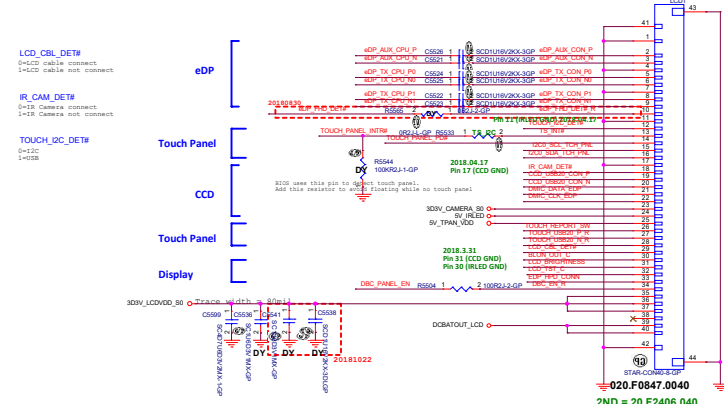
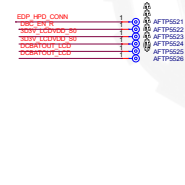
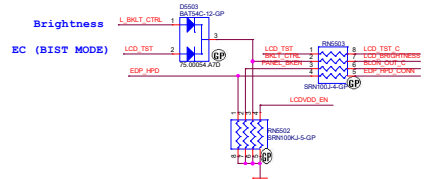
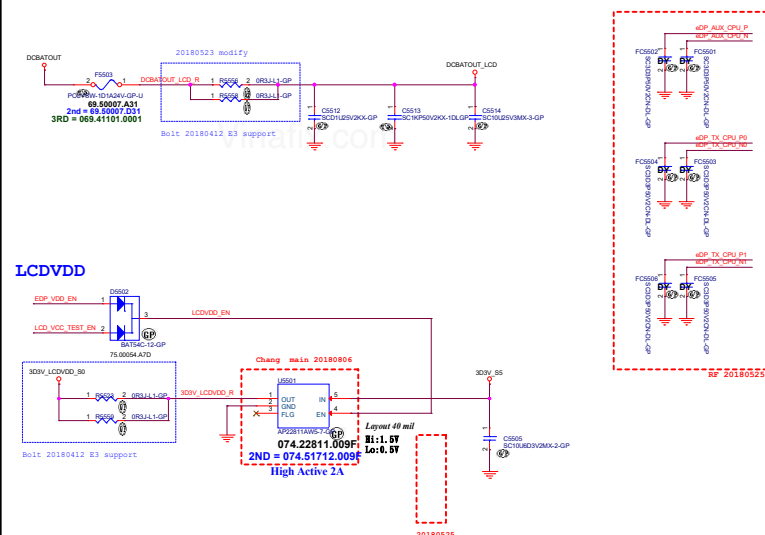


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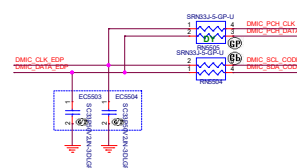
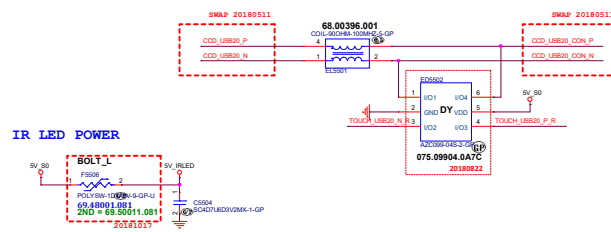
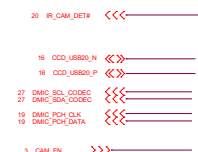
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Title (Reserved)			
Size A2	Document Number BOLT WHL		Rev 1
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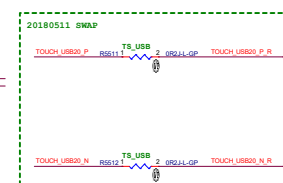
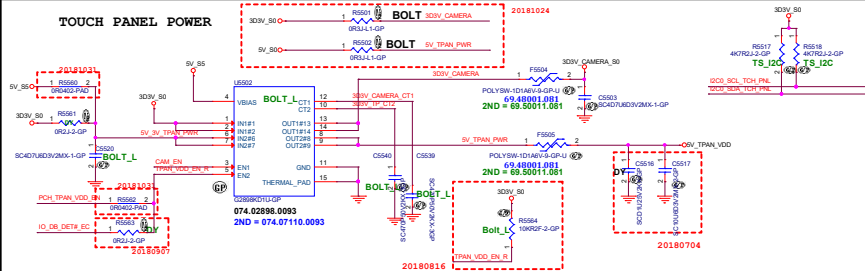
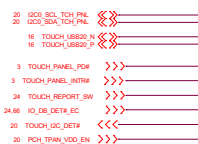
INVERTER POWER



Main Func = CAMERA

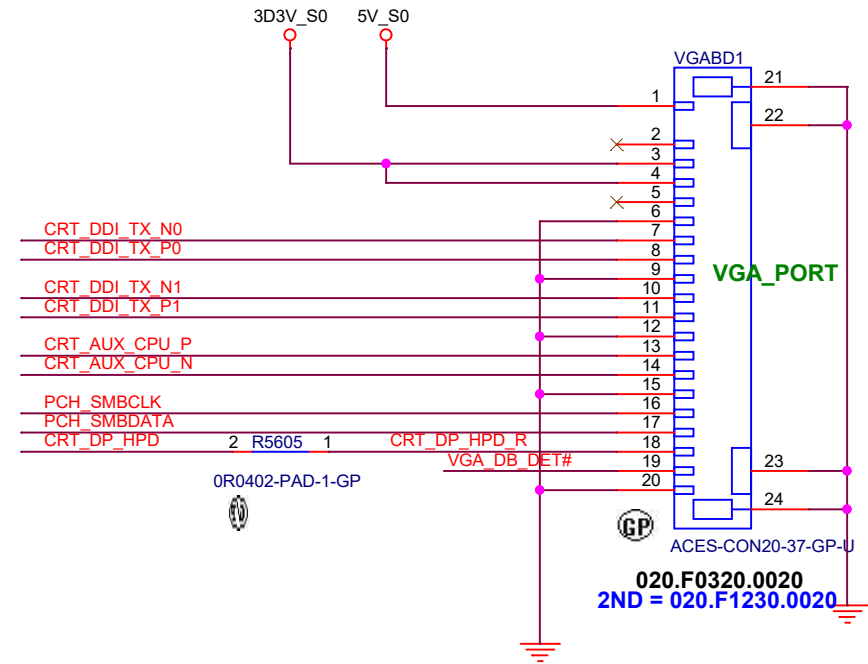
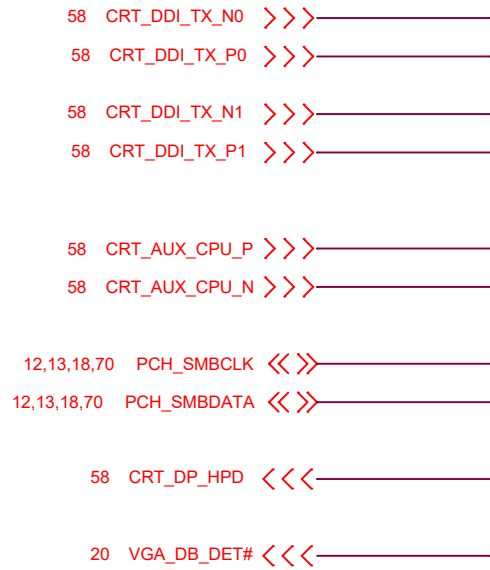


Main Func = Touch panel




Main Func = CRT

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Title CRT			
Size A4	Document Number BOLT WHL		Rev 1
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Main Func = DP Demux

CPU DP to DP De-MUX

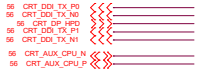


FOR Type C

From CCG:



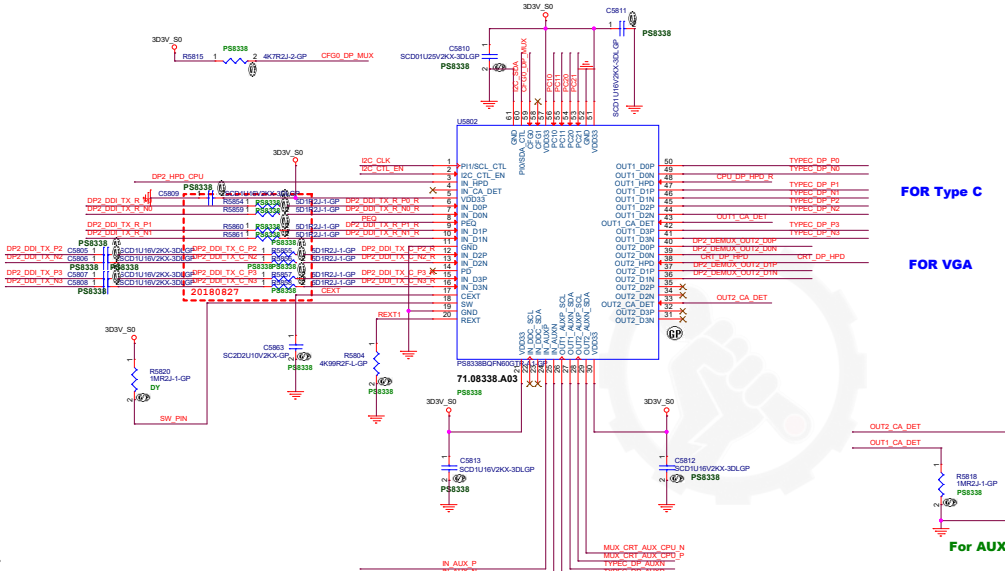
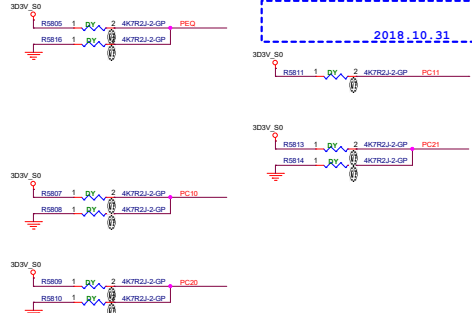
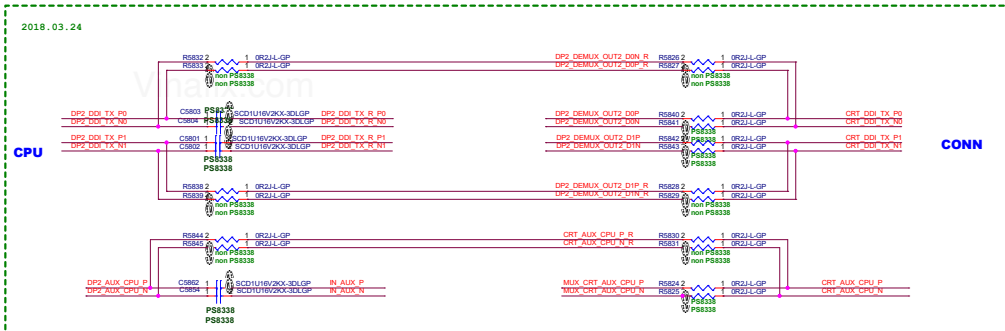
FOR VGA



24 GPU_THM_SMBDAT <<<<=====

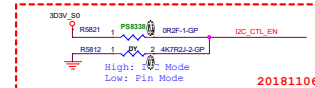
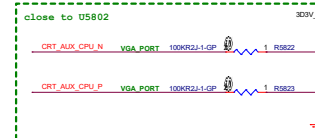
4 GPU_THM_SMBCLK <<<<=====

2018.10.31

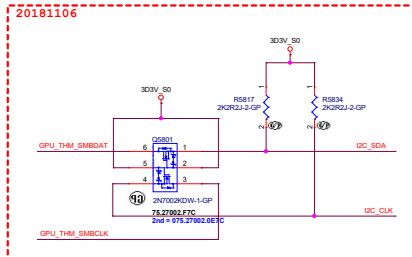


FOR Type C

FOR VGA



2018.10.31




SW	I/O	<p>Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O</p> <p>For Control Switching Mode (CFG0 = L):</p> <p>SW = L: Port1 is selected (default)</p> <p>SW = H: Port2 is selected</p> <p>For Automatic Switching Mode (CFG0 = H):</p> <p>SW = L: Port1 has higher priority when both ports are plugged (default)</p> <p>SW = H: Port2 has higher priority when both ports are plugged</p> <p>Overwritten by I2C control in I2C Control Mode</p>
----	-----	--



(Blanking)

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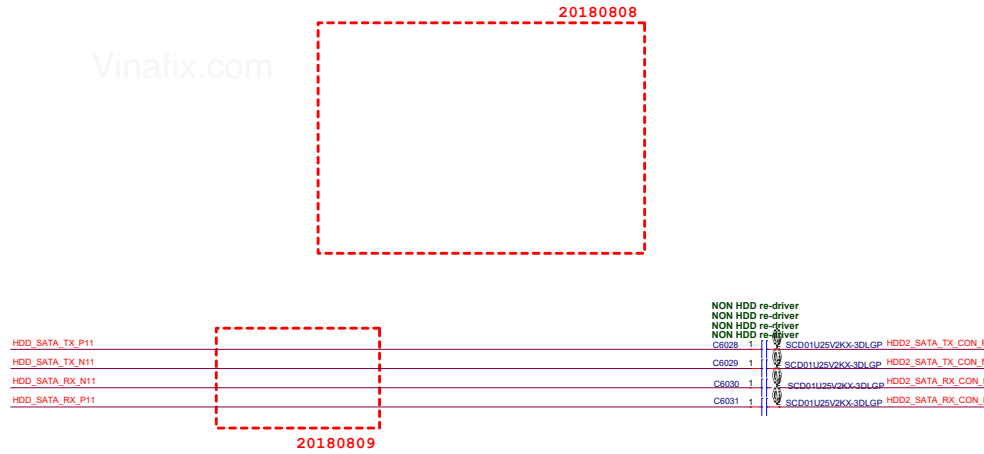
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number BOLT WHL		Rev 1
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Main Func = HDD

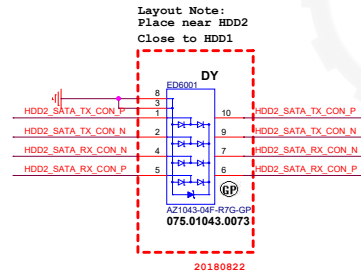
HDD

16 HDD_SATA_TX_P11 >>>
16 HDD_SATA_TX_N11 >>>
16 HDD_SATA_RX_P1 <<<
16 HDD_SATA_RX_N1 <<<
70 FFS_INT2_Q >>>
16 HDD_DEVSLP >>>
18,20 HDD_DET# <<<

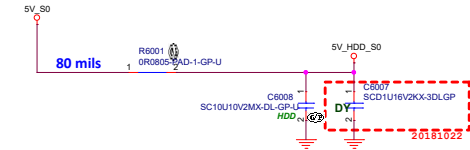
SATA RE-DRIVER



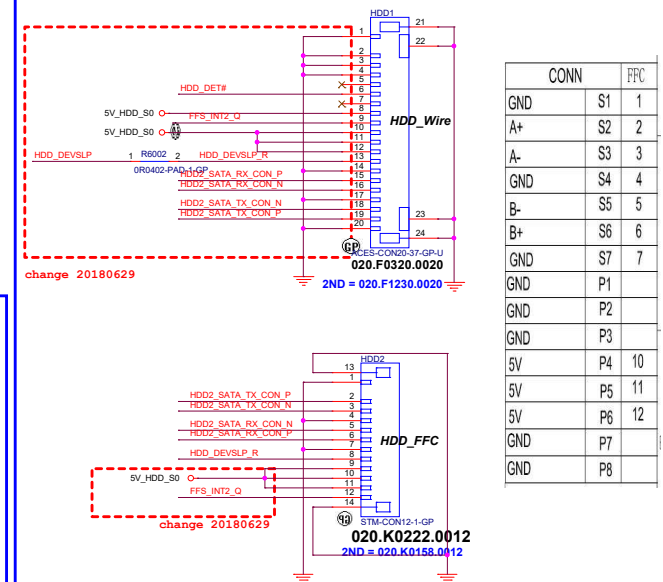
HDD ESD



HDD POWER



SATA HDD Connector

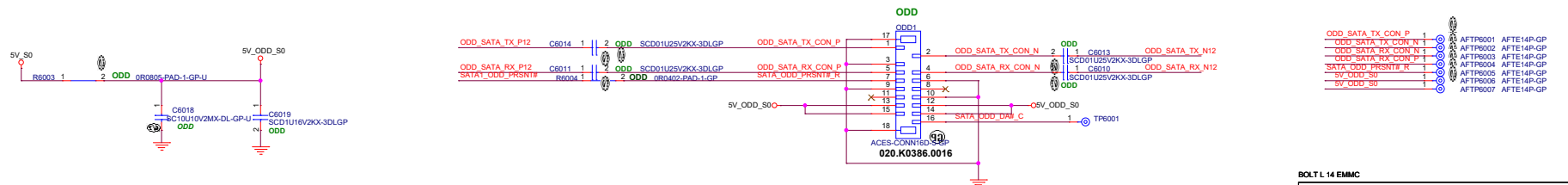


Main Func = ODD

ODD

16 ODD_SATA_TX_P12 >>>
16 ODD_SATA_TX_P12 >>>
16 ODD_SATA_RX_P12 <<<
16 ODD_SATA_RX_P12 <<<
16 SATA1_ODD_PRSNT# >>>

ODD Connector



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Taipexi Hsien 221, Taiwan, R.O.C.

Title **SATA IF HDD/ODD**
BOLT WHL
Size A0 Document Number
Date: Friday, December 28, 2018 Sheet 50 of 105

Main Func = WLAN

BT

21 BLUETOOTH_EN >>>
16 BT_USB20_N >>>
16 BT_USB20_P >>>

WLAN

18 CLK_PCIE_WLAN_REG# >>>
18 WLAN_CLK_CPU_N >>>
18 WLAN_CLK_CPU_P >>>
16 WLAN_PCIE_RX_N10 >>>
16 WLAN_PCIE_RX_P10 >>>
16 WLAN_PCIE_TX_N10 >>>
16 WLAN_PCIE_TX_P10 >>>

CNVI

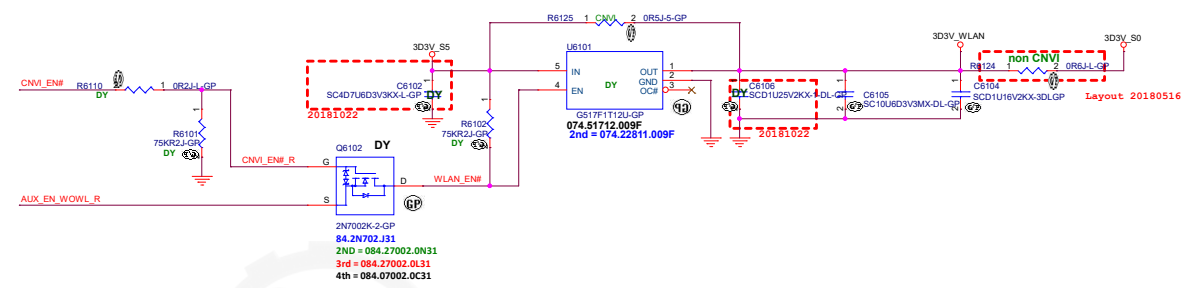
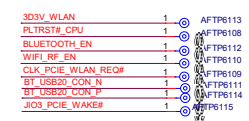
19 BT_PCMFRM_RSTN >>>
19 BT_PCMOUT_CLKREQ0 >>>
18 PULSAR_384M_REFCLK >>>
20 CNV_RGI_RSP >>>
15,20 CNV_RGI_DT_R >>>
20 CNV_BRI_RSP >>>
20 CNV_BRI_DT_R >>>
21 CNV_WT_CLK_DP >>>
21 CNV_WT_CLK_DN >>>
21 CNV_WT_DP0 >>>
21 CNV_WT_DN0 >>>
21 CNV_WT_DP1 >>>
21 CNV_WT_DN1 >>>
21 CNV_WR_CLK_DP >>>
21 CNV_WR_CLK_DN >>>
21 CNV_WR_DP0 >>>
21 CNV_WR_DN0 >>>
21 CNV_WR_DP1 >>>
21 CNV_WR_DN1 >>>

Others

18,24 SUS_CLK >>>
4 CNV_EN# >>>
17,24 AUX_EN_WOVL_R >>>
17,18,24 J03_PCIE_WAKE# <<<
21 WIFI_RF_EN >>>
17,26,31,62,63,91 PLTRST#_CPU >>>

CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN

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Main Func = WWAN

19,24 WWAN_DB_DET# <<<_____

24 INT#_ITE8010 << >> _____
24 CLK_ITE8010 << >> _____
24 DAT_ITE8010 << >> _____

WWAN

```

16 WWAN_PCIE_RX_N  << >> _____
16 WWAN_PCIE_RX_P  << >> _____
16 WWAN_PCIE_TX_N  << >> _____
16 WWAN_PCIE_TX_P  << >> _____

```

```

18 WWAN_CLKREQ_CPU_N <<< _____
18 WWAN_PCIE_CLK_P   >>> _____
18 WWAN_PCIE_CLK_N   >>> _____

```

16 WWAN_USB20_N << >> _____
16 WWAN_USB20_P << >> _____

17,26,31,61,63,91 PLTRST#_CPU >>>_____

```

>>WWAN_BB_RST# 21

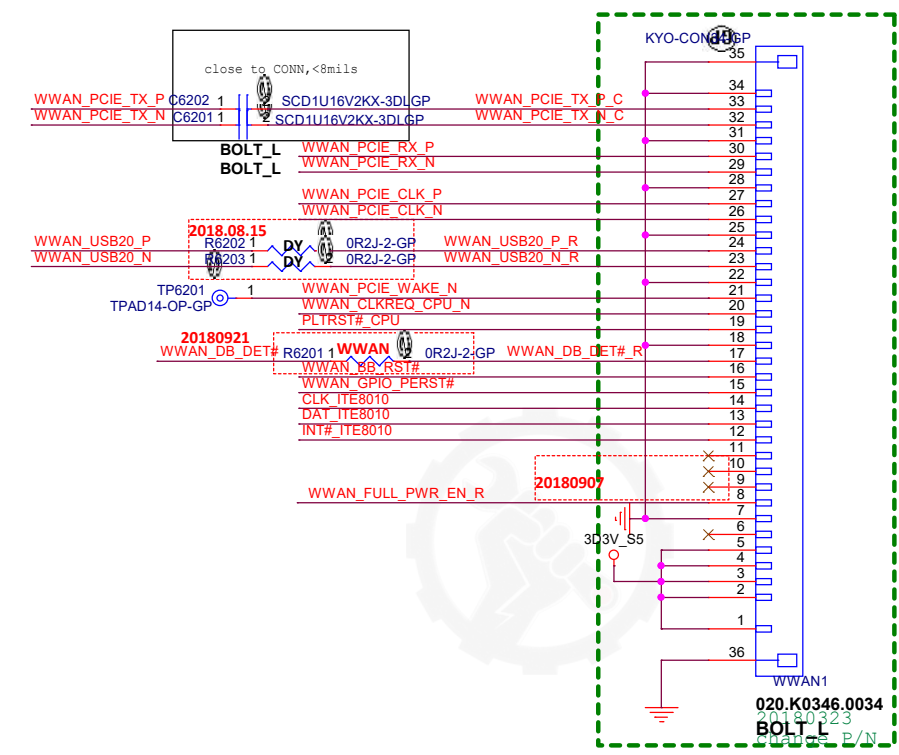
```

```
>>> WWAN_FULL_PWR_EN_R 20
```

```

->>> WWAN_GPIO_PERST# 20

```



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	Title
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WWAN

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Custom	

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1

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7,26,31,8



7,26,31,8

7,26,31,8

7,26,31,8

7,26,31,8

7,26,31,8

7,26,31,8



7,26,31,8

7,26,31,8

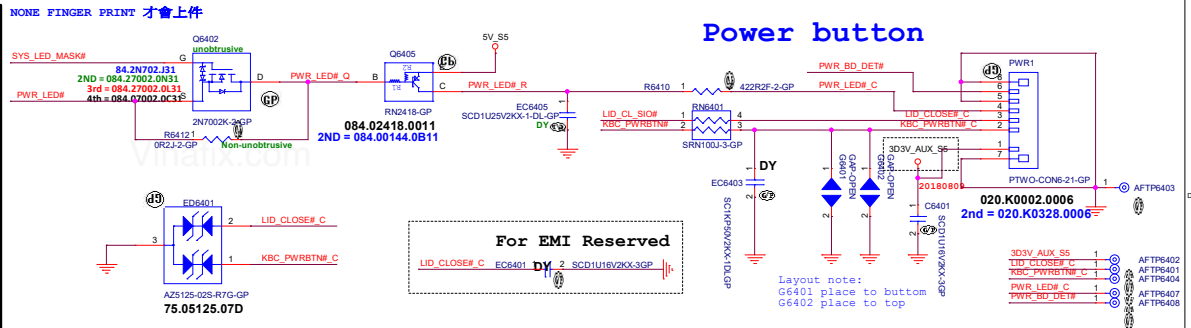
7,26,31,8

7,26,31,8

7,26,31,8

Main Func = Power BTN

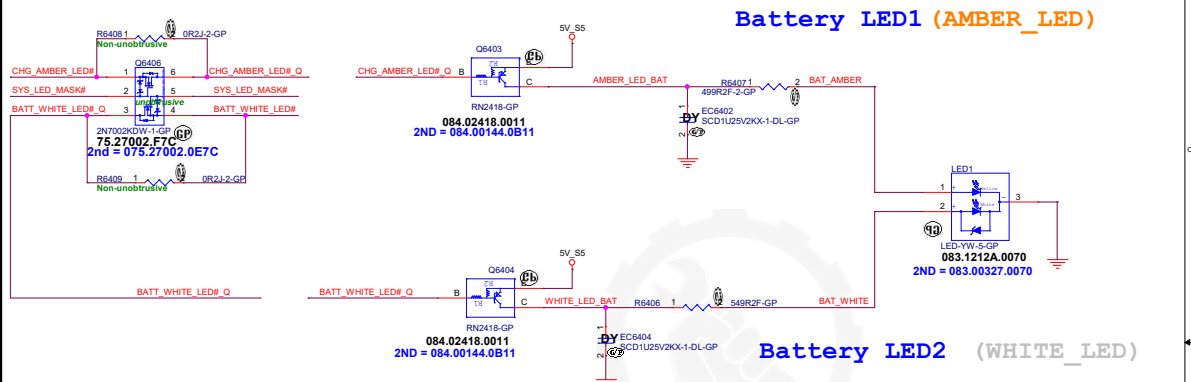
24 PWR_LED# >>> _____
20.21 PWR_BD_DET# <<< _____
24.92 LID_CL_SIO# <<< _____
24.92 KBC_PWRBTN# <<< _____



Main Func = Battery LED

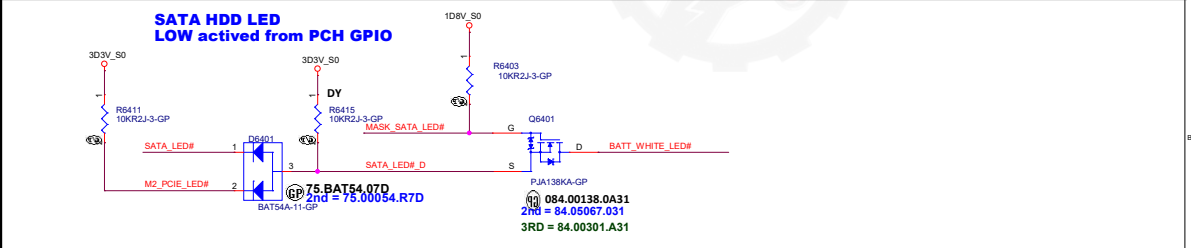
Low activated from KBC GPIO

24.32 SYS_LED_MASK# >>> _____
24 CHG_AMBER_LED# >>> _____
24 BATT_WHITE_LED# >>> _____



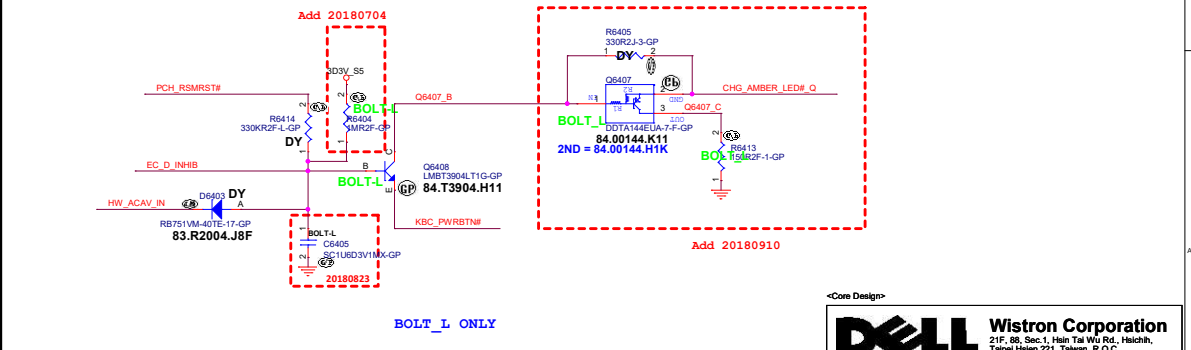
Main Func = HDD LED

24 MASK_SATA_LED# >>> _____
16 SATA_LED# >>> _____
63 M2_PCIE_LED# <<< _____



Main Func = M-BIST

17.24 PCH_RSMRST# >>> _____
24 EC_D_IN#B >>> _____
24.43.44 HW_ACAV_IN >>> _____



Main Func = KB

24 CAP_LED#_R >>> _____

24 KSI[0..7] >>> _____

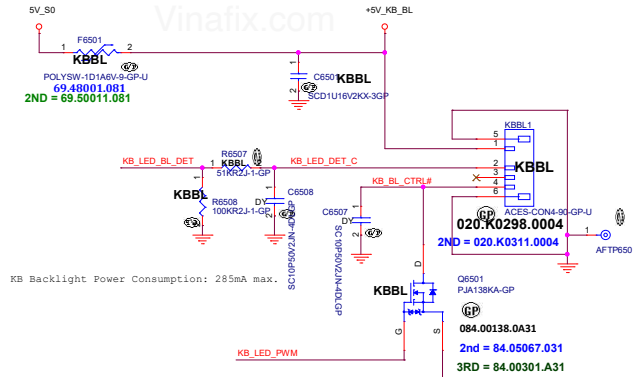
24 KSO[0..16] <<< _____

20 KB_DET# <<< _____

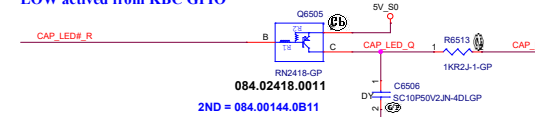
19 KB_LED_BL_DET <<< _____

24 KB_LED_PWM >>> _____

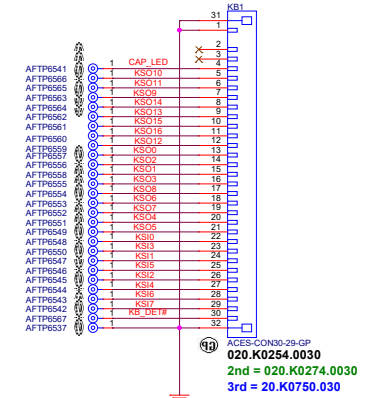
Keyboard Backlight (Reserved)



CAP LED Control LOW active from KBC GPIO



Internal Keyboard Connector



Main Func = TPAD

24 TP_EN# >>> _____

24 CLK_TP_SIO <<< _____

24 DAT_TP_SIO <<< _____

20 I2C0_SCL_TCH_PAD <<< _____

20 I2C0_SDA_TCH_PAD <<< _____

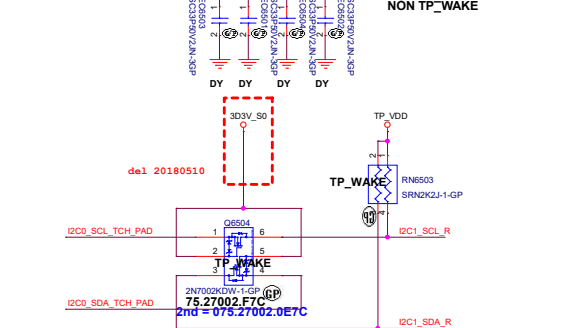
3,24 TP_WAKE_KBC# <<< _____

24 PTP_DIS# >>> _____

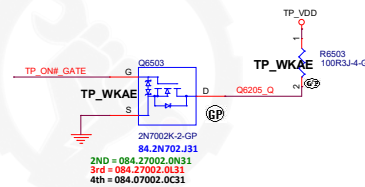
Support PTP

PS2

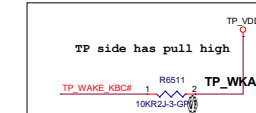
I2C



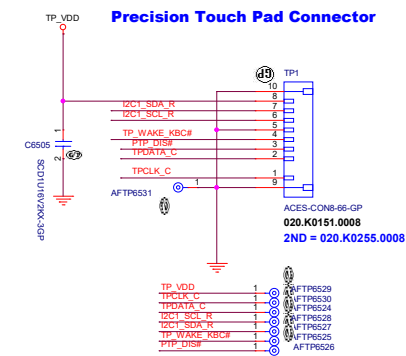
TP_VDD Discharge Circuit



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Precision Touch Pad Connector

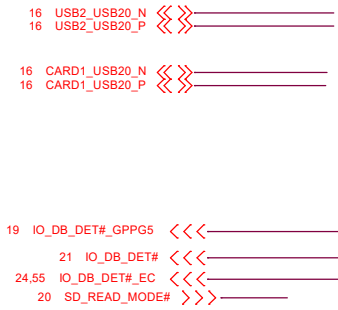


Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

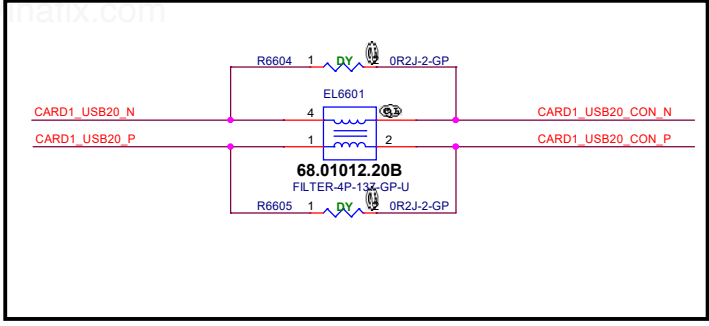
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Main Func = IO Connector

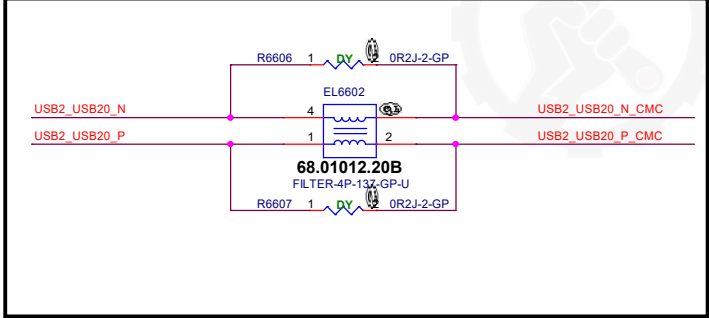
USB 2.0



USB2.0 CARD



USB2.0



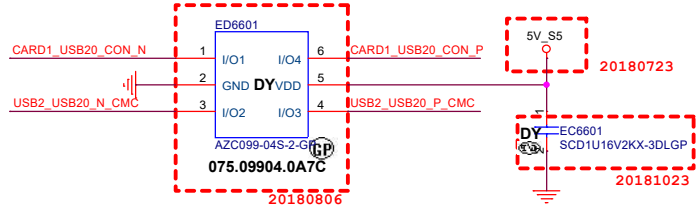
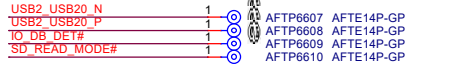
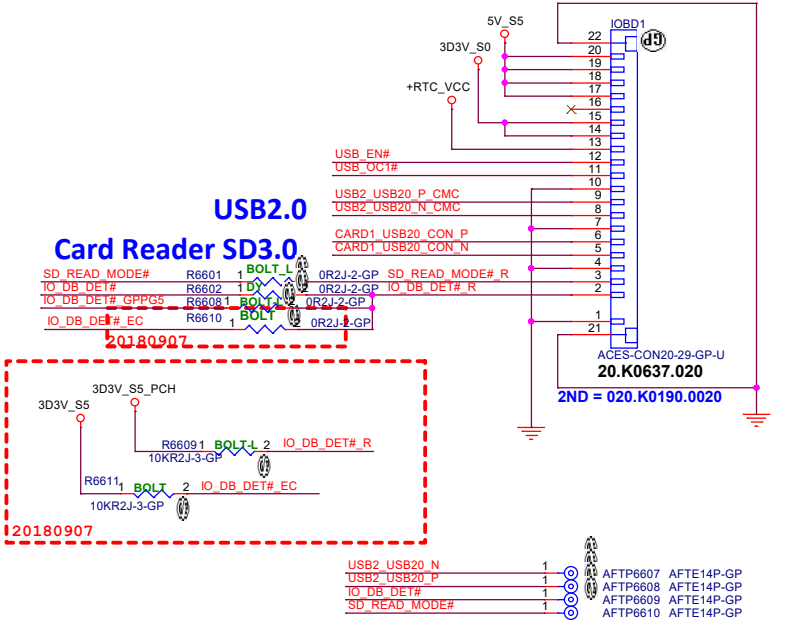
USB OC



USB Switch Enable




USB2.0 Card Reader SD3.0



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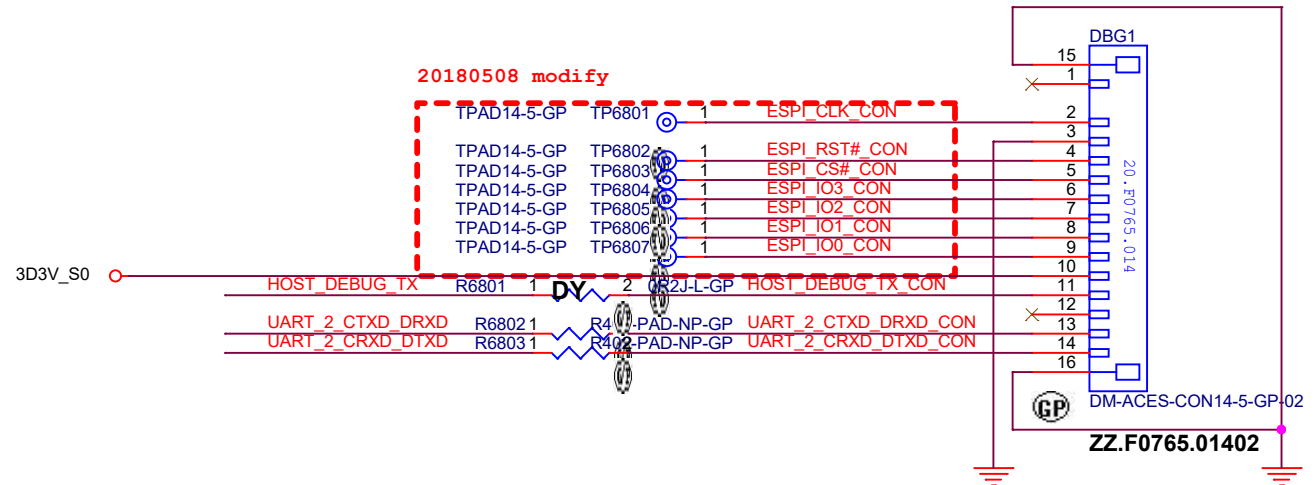
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Title			
<i>Reserved</i>			
Size A4	Document Number BOLT WHL		Rev 1
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Main Func = Debug

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Debug Connector

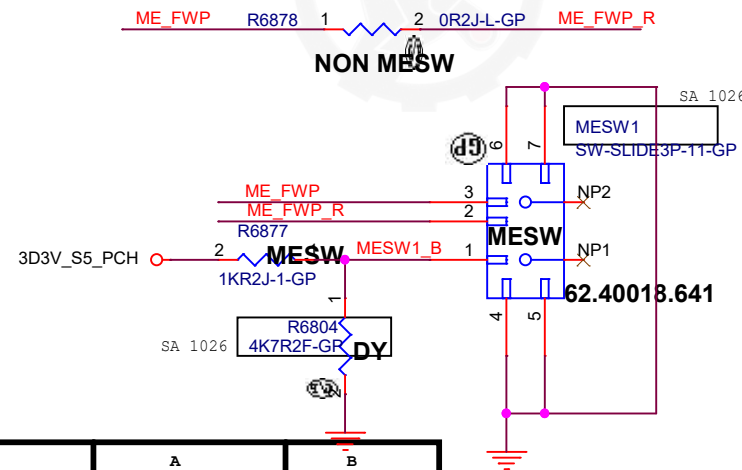


24 HOST_DEBUG_TX >>>—

20 UART_2_CTXD_DRXD <<<—

20 UART_2_CRXD_DTXD <<<—

Firmware SW



24 ME_FWP <<<—

19 ME_FWP_R <<<—

MESW1_B 1 AFTP6801 AFTE14P-GP

ME_FWP_R 1 AFTP6802 AFTE14P-GP

ME_FWP 1 AFTP6803 AFTE14P-GP

	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override

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Title

Dubug connector

Size
A4

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<i>Reserved</i>			
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Main Func = Free Fall Sensor

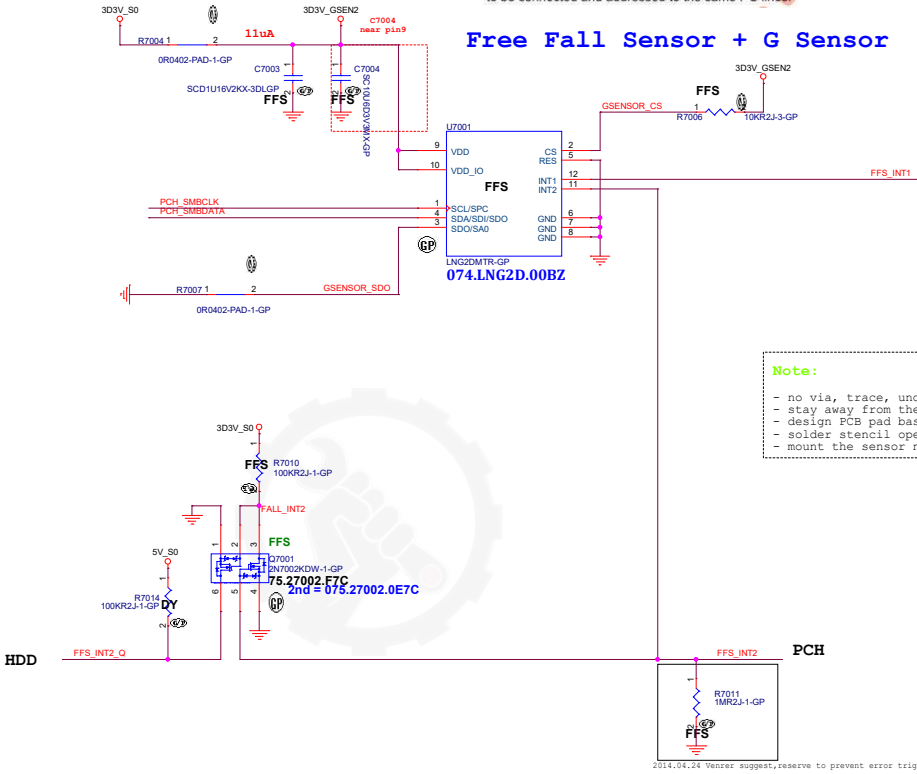
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12,13,18,56	PCH_SMBDATA	<< >>	_____
12,13,18,56	PCH_SMBCLK	<< >>	_____

18 FFS_INT1 <<<—
20 FFS_INT2 <<<—
60 FFS_INT2_Q <<<—

The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

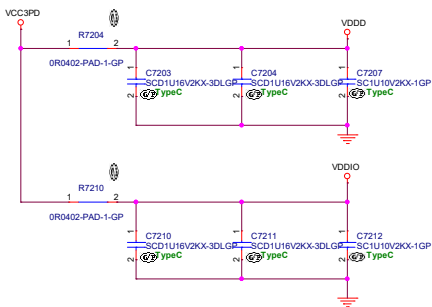
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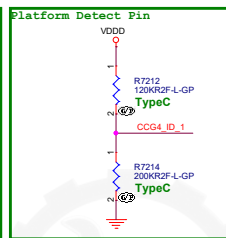
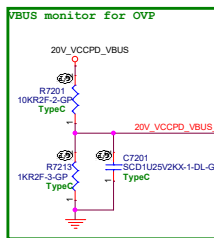
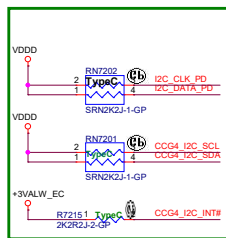
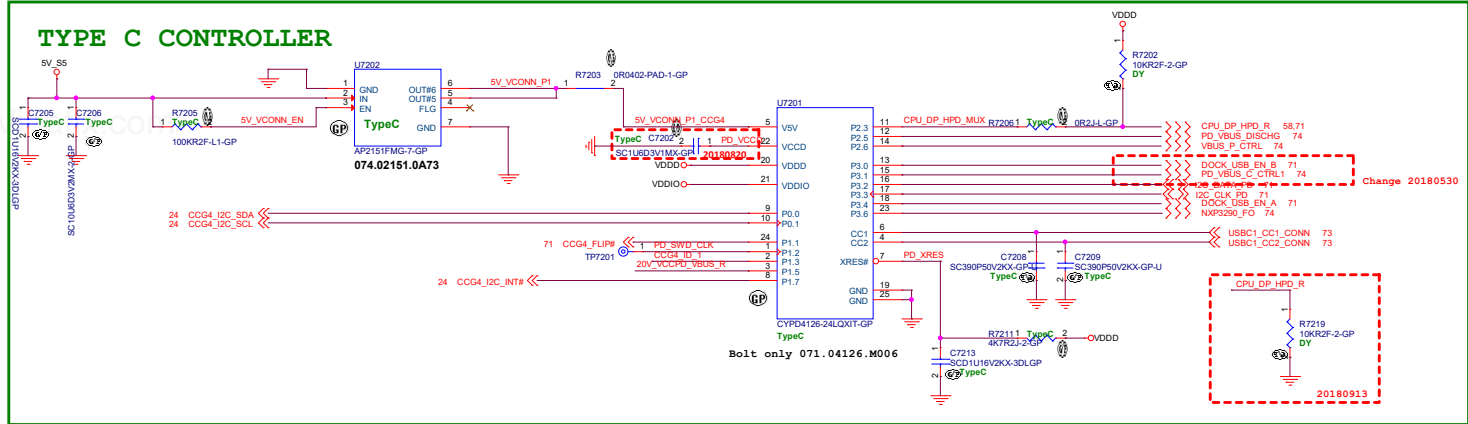
Title			
(Reserved)			
Size A2	Document Number	Rev	
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Main Func = TYPEC CONTROLLER

Power

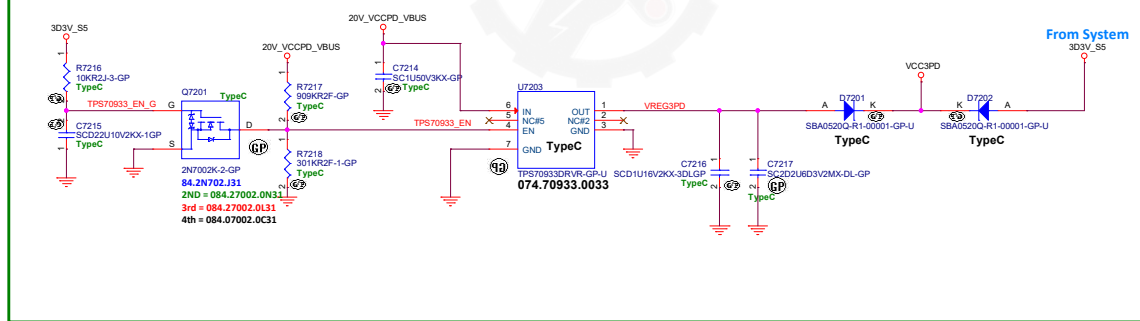


TYPE C CONTROLLER



S.No	Project Name	ODM	CCG4 ID 1	Single/ Dual Port	Port 1 Configuration	Port 2 Configuration	Voltage level	Voltage value
1	Bolt (WHL) Data Only with PS8743B Mux	Wistron	L0	Single	USB	N/A	L0	0V
2	Bolt (WHL) Data Only with TUSB546 Mux	Wistron	L1	Single	USB	N/A	L1	3.3V/8
3	Bolt (CNL) Data Only with PS8743B Mux	Wistron	L2	Single	USB	N/A	L2	2 * 3.3V/8
4	Bolt (CNL) Data Only with TUSB546 Mux	Wistron	L3	Single	USB	N/A	L3	3 * 3.3V/8
5	Bolt (WHL) Full Feature with PS8743B Mux	Wistron	L4	Single	USB+DP+ PD Charging	N/A	L4	4 * 3.3V/8
6	Bolt (WHL) Full Feature with TUSB546 Mux	Wistron	L5	Single	USB+DP+ PD Charging	N/A	L5	5 * 3.3V/8
7	Bolt (CNL) Full Feature with PS8743B Mux	Wistron	L6	Single	USB+DP+ PD Charging	N/A	L6	6 * 3.3V/8
8	Bolt (CNL) Full Feature with TUSB546 Mux	Wistron	L7	Single	USB+DP+ PD Charging	N/A	L7	7 * 3.3V/8

For Dead Battery modify



	CCG4 ID 1	R7212	R7214	計算値	理論値
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1		64.71535.06D1 (715K)	0.123	0.125
2/8	L2		64.30035.6DL (300K)	0.25	0.25
3/8	L3		64.20035.6DL (200K)	0.375	0.375
4/8	L4		64.10035.6DL (100K)	0.5	0.5
5/8	L5		64.12035.6DL (120K)	0.625	0.625
6/8	L6		64.22035.6DL (220K)	0.728	0.75
7/8	L7		64.10035.6DL (100K)	0.877	0.875

Core Design

DELL Wistron Corporation
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsinshih,
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Title: **USB3.0 PORT**

Size: Custom Document Number: **BOLT WHL** Rev: **1**

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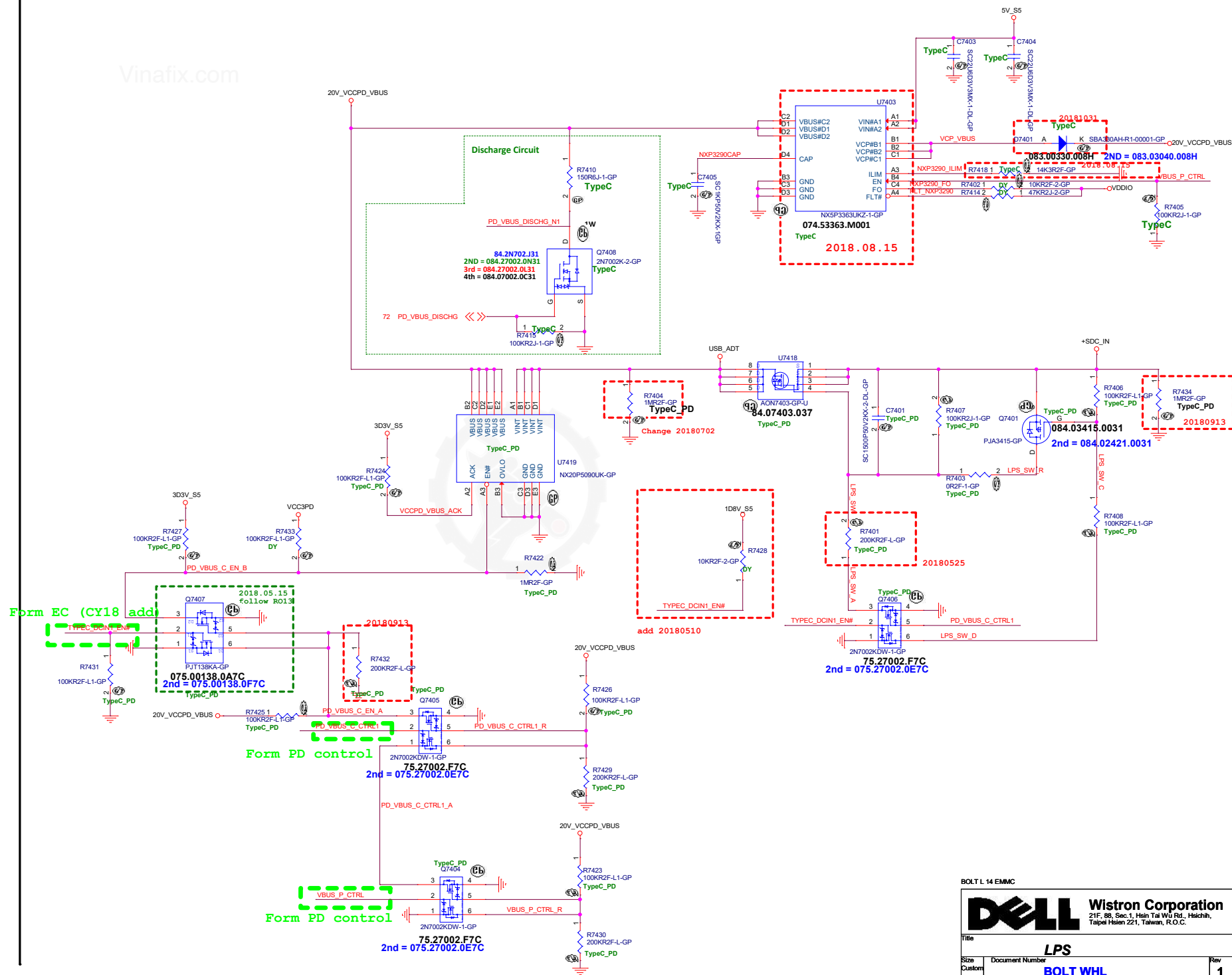
Main Func = LPS

```

72 PD_VBUS_C_CTRL1 >>>_____
72 VBUS_P_CTRL >>>_____
24 TYPEC_DCIN1_EN# >>>_____
72 NXP3290_FO <<<_____

```

44 VCCPD_VBUS_ACK >>_____



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Title			
LPS			
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Title (Reserved)			
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Title

GPU(1/5)PEG

Size

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Title			
GPU(2/5)DIGITALOUT			
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File			
GPU(3/5)VRAM/F			
Revision Number			
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			1
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Title		GPU(5/5)PWR/GND	
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Title		GPU-VRAM1,2 (1/4)	
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipai Hsien 221, Taiwan, R.O.C.	
Title		GPU-VRAM3.4 (2/4)	
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Title			
GPU-VRAM5,6 (3/4)			
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Title			GPU-VRAM7,8 (4/4)	
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VGA Power B
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		22F, 4F, 5F, 1F, 2F, 3F, 4F, 5F, 6F, 7F, 8F, 9F, 10F, 11F, 12F, 13F, 14F, 15F, 16F, 17F, 18F, 19F, 20F, 21F, 22F, 23F, 24F, 25F, 26F, 27F, 28F, 29F, 30F, 31F, 32F, 33F, 34F, 35F, 36F, 37F, 38F, 39F, 40F, 41F, 42F, 43F, 44F, 45F, 46F, 47F, 48F, 49F, 50F, 51F, 52F, 53F, 54F, 55F, 56F, 57F, 58F, 59F, 60F, 61F, 62F, 63F, 64F, 65F, 66F, 67F, 68F, 69F, 70F, 71F, 72F, 73F, 74F, 75F, 76F, 77F, 78F, 79F, 80F, 81F, 82F, 83F, 84F, 85F, 86F, 87F, 88F, 89F, 90F, 91F, 92F, 93F, 94F, 95F, 96F, 97F, 98F, 99F, 100F	
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緯創資通

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DISCRETE VGA POWER		
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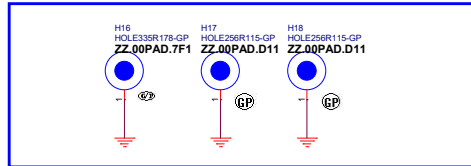
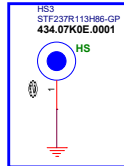
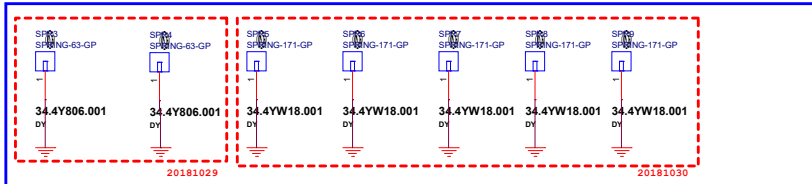
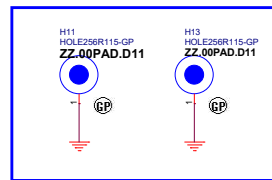
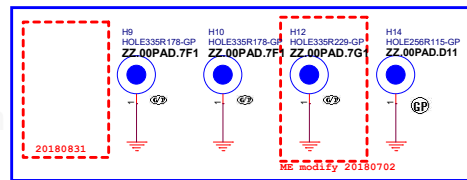
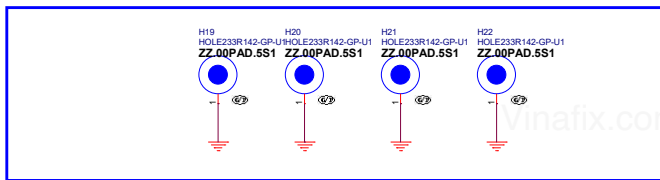
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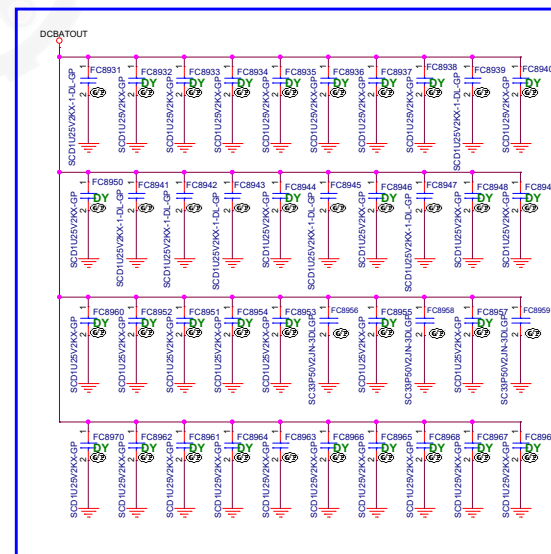
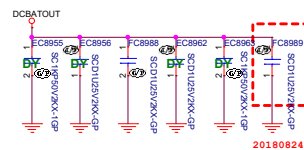
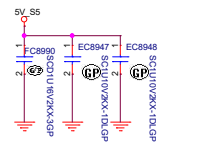
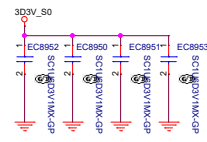
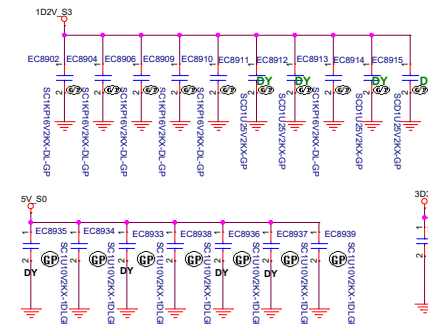
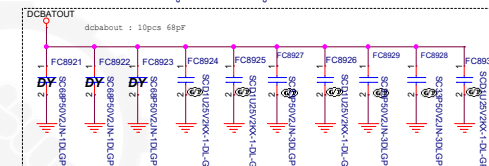
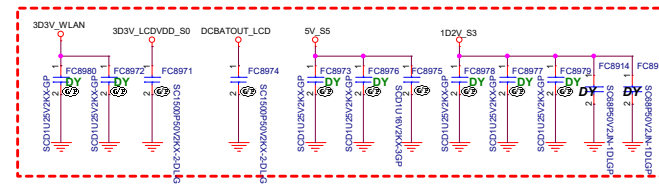
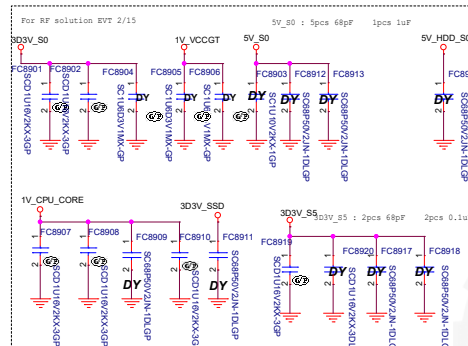
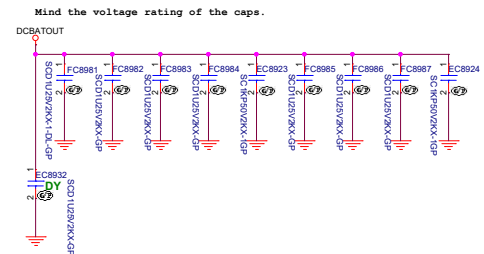
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Title			
GPU SEQUENCE			
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Main Func = UnusedParts



Main Func = EMI & RF Capacitors




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File			
UNUSED PARTS/EMI Capacitors			
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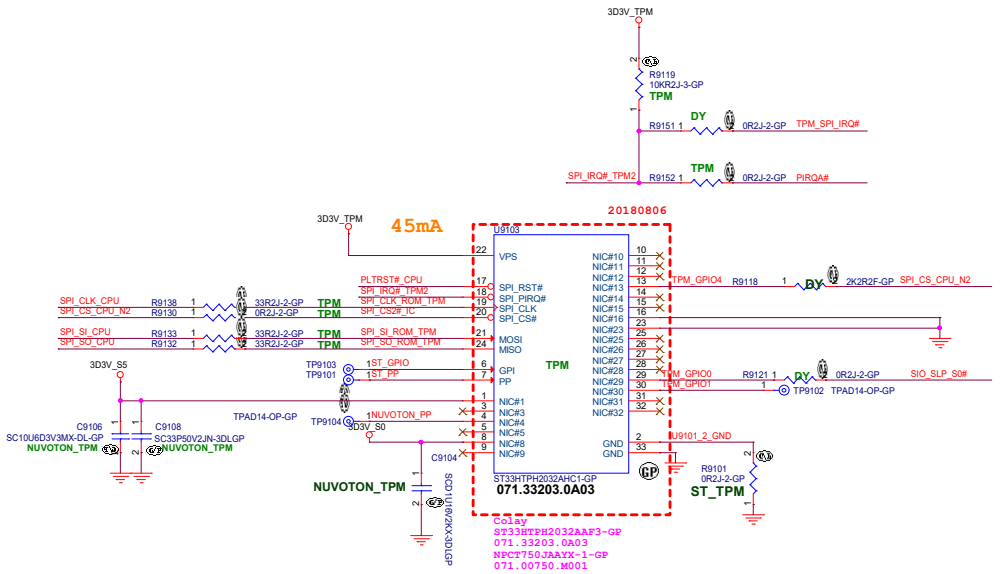
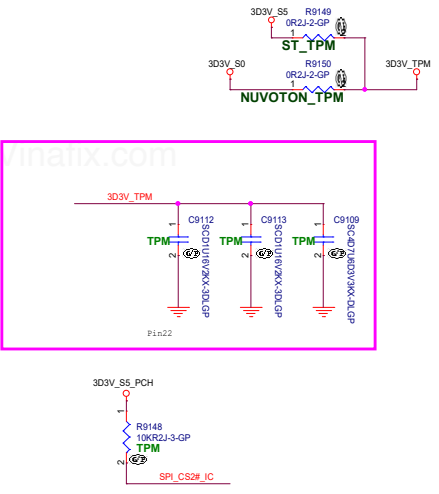
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Main Func = TPM

- 18,25 SPI_SO_CPU <<<
- 18,25 SPI_CLK_CPU >>>
- 15,18,25 SPI_SI_CPU >>>
- 18 SPI_CS_CPU_N2 <<<
- 17,26,31,61,62,63 PLTRST#_CPU >>>
- 17,40 SIO_SLP_S0# >>>
- 20 PIRQA# <<<
- 18 TPM_SPI_IRQ# <<<



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

BOLT L 14 EMMC



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Title

TPM2.0

Size

Document Number

Rev

Custom

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1

Date

Friday, December 28, 2018

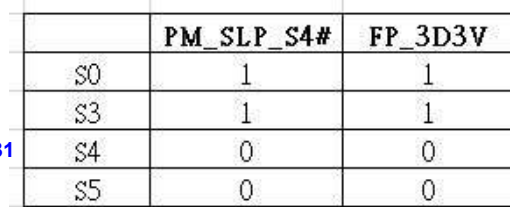
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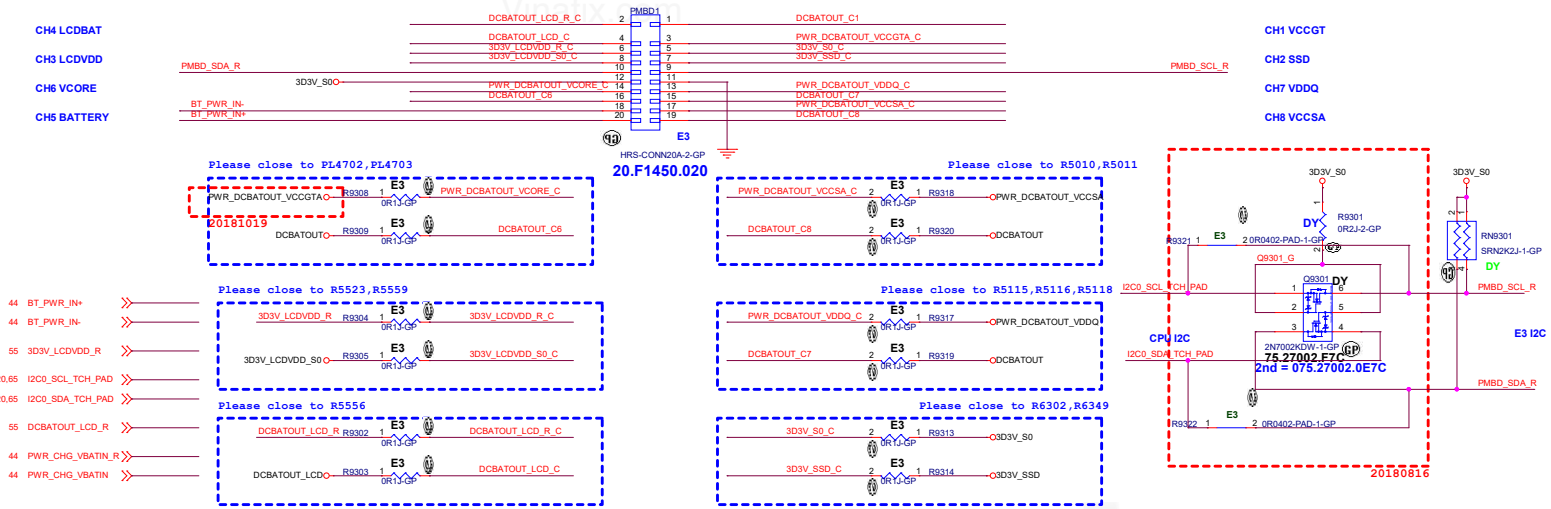
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FBR(Botton side finger Print Sensor)

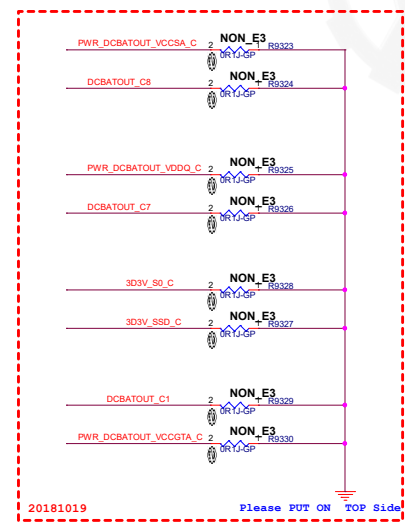
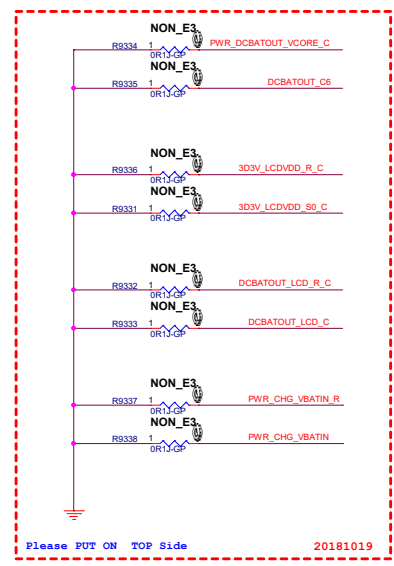


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Main Func = E3



- 44 BT_PWR_IN+ >>>
- 44 BT_PWR_IN- >>>
- 55 3D3V_LCDVDD_R >>>
- 20.65 I2C0_SCL_TCH_PAD >>>
- 20.65 I2C0_SDA_TCH_PAD >>>
- 55 DCBATOUT_LCD_R >>>
- 44 PWR_CHG_VBATIN_R >>>
- 44 PWR_CHG_VBATIN >>>



WHL	
P1+/-	CPU_VCCGT (iGPU Core) <input>
P2+/-	STORAGE (SSD/HDD) <output>
P3+/-	DISPLAY_CTLR <output>
P4+/-	DISPLAY_BACKLIGHT <output>
P5+/-	SYSTEM (battery leads)
P6+/-	CPU_VCORE <input>
P7+/-	CPU_VDDQ (MCU Core) <input>
P8+/-	CPU_VCCSA (PCH Core) <input>

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

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Title			
LVDS_Switch			
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Main Func = Firmware SW

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Title

Firmware SW

Size
A4

Document Number
BOLT WHL

Rev
1

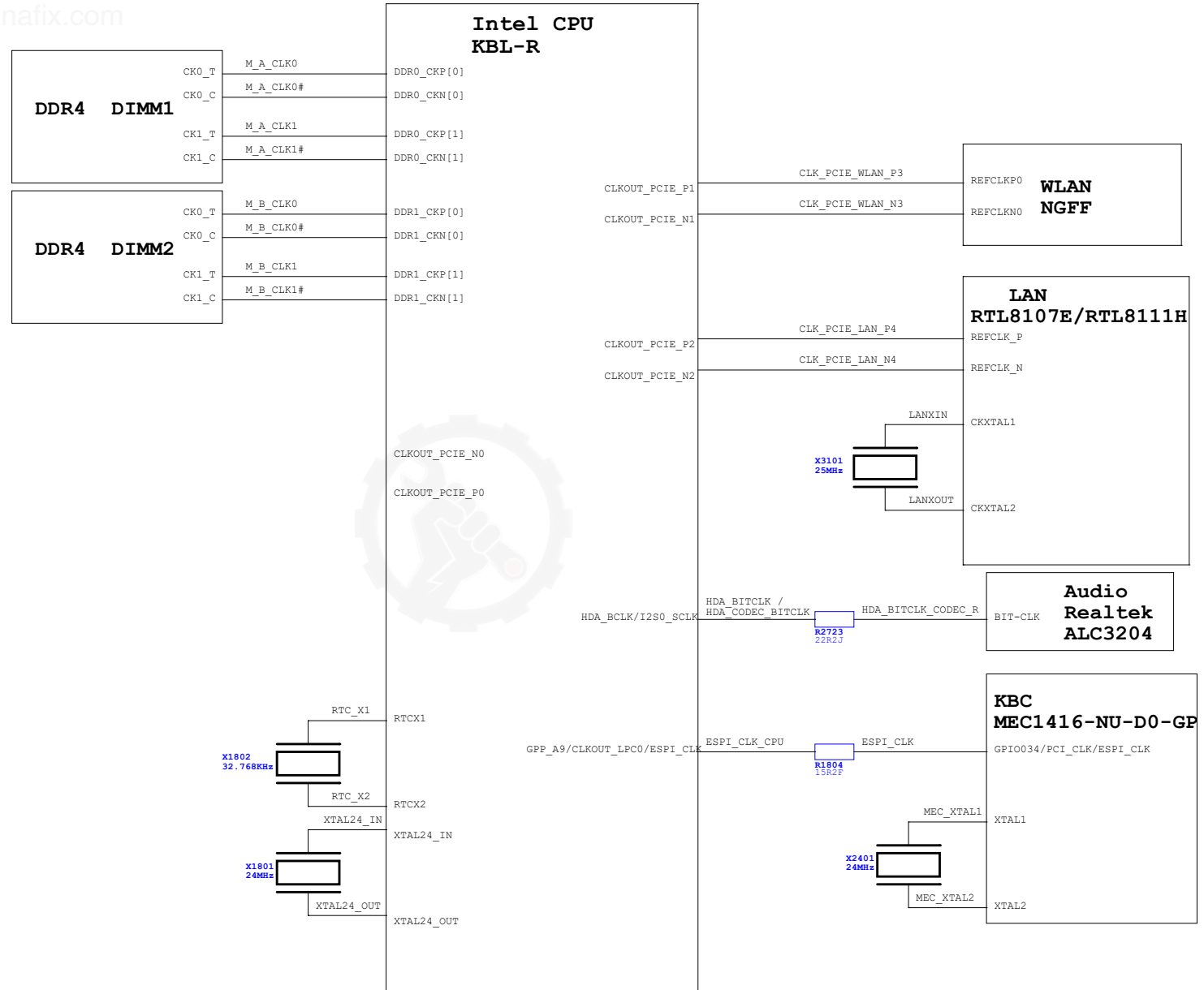
Date: Thursday, December 27, 2018

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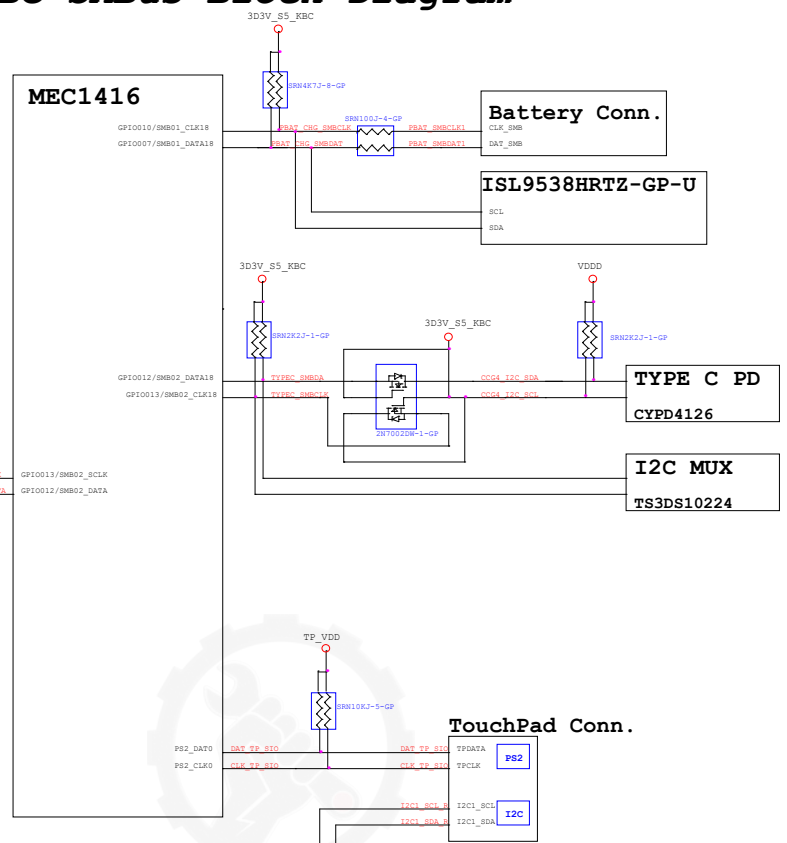
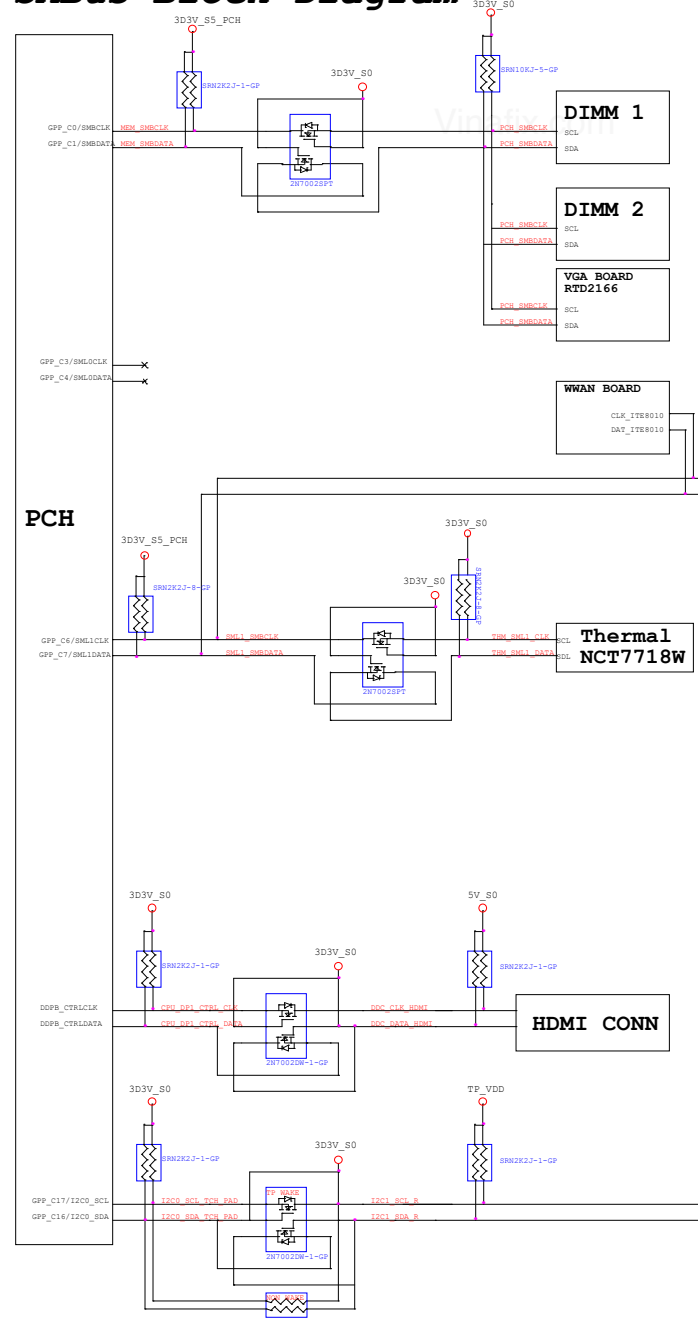
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Title <i>Change History</i>	
Size A3	Document Number Rev 1
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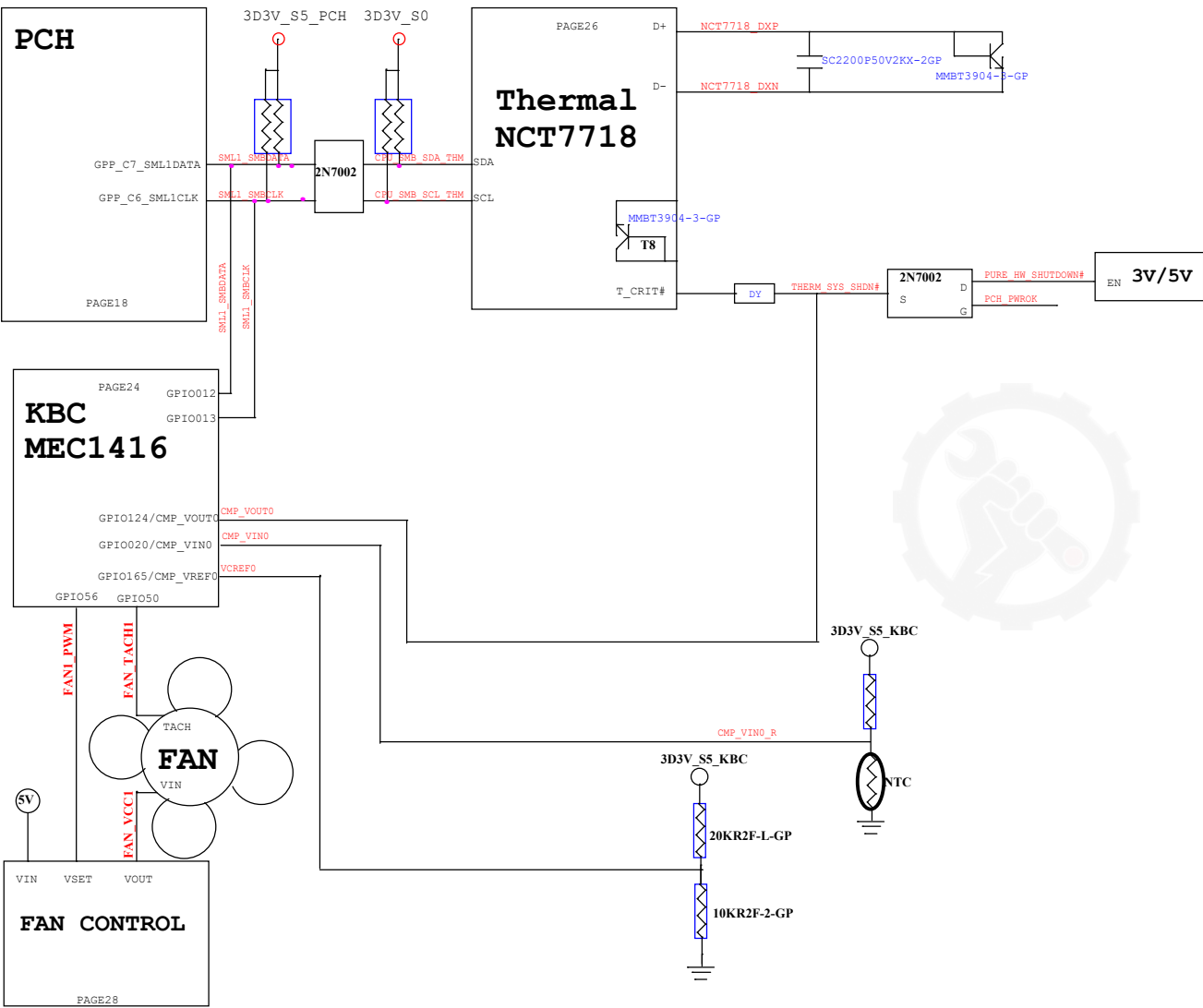
PCH SMBus Block Diagram

KBC SMBus Block Diagram



Thermal Block Diagram

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Audio Block Diagram

